POLYTECHNIC 2nd SEMESTER

Fundamentals of Electrical & Electronics Engineering

CHAPTER NOTES

OVERVIEW OF BASIC SEMICONDUCTOR DEVICES

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2. Intrinsic & Extrinsic Semiconductors, Doping, P-Type and N-Type
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1. Energy Level Diagrams of Insulator, Conductor & Semiconductor

1.1 Concept of Energy Bands

In solid materials, electrons do not occupy single discrete energy levels as in isolated atoms. Instead, due to the close proximity of a large number of atoms in a solid, the individual energy levels of electrons split and merge into groups called energy bands. The two most important energy bands are:

- **Valence Band:** Valence Band
- The highest energy band that is completely filled with electrons at 0 K (absolute zero). Electrons in this band are bound to their parent atoms and do not participate in conduction under normal conditions.
- **Conduction Band:** Conduction Band
- The energy band above the valence band. Electrons in this band are free to move throughout the material and can participate in electrical conduction.

The Forbidden Energy Gap (Eg)

Between the valence band and the conduction band, there exists a region where no electron can exist under normal conditions. This region is called the Forbidden Energy Gap or Band Gap (Eg). The width of this gap — measured in electron-volts (eV) — is the most important factor that determines whether a material is an insulator, semiconductor, or conductor.

$$1\ eV = 1.6 \times 10^{-19}\ Joules$$

Unit of energy gap

1.2 Energy Band Diagrams

INSULATOR	SEMICONDUCTOR	CONDUCTOR
Conduction Band (Empty)	Conduction Band (Partially filled at room temp)	Conduction Band (Overlaps Valence Band)
Large Forbidden Gap (> 5 eV)	Small Forbidden Gap (0.7 - 1.1 eV)	No Forbidden Gap (Bands overlap)
Valence Band (Full)	Valence Band (Full at 0K)	Valence Band (Full)
Example: Glass, Rubber (Eg > 5 eV)	Example: Si (1.1 eV), Ge (0.67 eV)	Example: Copper, Aluminium

(a) Insulator

In insulators, the valence band is completely filled and the conduction band is completely empty. The forbidden energy gap between the two bands is very large — typically greater than 5 eV. At room

temperature, electrons in the valence band cannot gain enough thermal energy to jump across this large gap into the conduction band. Therefore, insulators do not conduct electricity under normal conditions.

- Examples: Glass, Rubber, Wood, Diamond (Eg ≈ 6 eV), Mica
- Forbidden gap: Greater than 5 eV
- Electrical conductivity: Extremely low (practically zero)

(b) Conductor

In conductors, the valence band and the conduction band overlap — there is no forbidden energy gap. This means that even at 0 K, a large number of free electrons are already present in the conduction band. These electrons can move freely under the influence of even a very small electric field, making conductors excellent carriers of electricity.

- Examples: Copper, Aluminium, Silver, Gold
- Forbidden gap: Zero (bands overlap)
- Electrical conductivity: Very high (10^6 to 10^7 S/m)

(c) Semiconductor

Semiconductors have a small forbidden energy gap — typically between 0.1 eV and 3 eV. At absolute zero (0 K), a semiconductor behaves like an insulator because the valence band is full and the conduction band is empty. However, at room temperature (300 K), some electrons gain enough thermal energy to jump across the small forbidden gap into the conduction band, leaving behind positively charged vacancies called holes. Both electrons and holes contribute to the electrical conductivity of the semiconductor.

- Examples: Silicon (Eg = 1.1 eV), Germanium (Eg = 0.67 eV), Gallium Arsenide (Eg = 1.43 eV)
- Forbidden gap: 0.1 eV to 3 eV
- Conductivity increases with temperature (negative temperature coefficient)

Key Insight: As temperature increases, more electrons jump the forbidden gap in semiconductors, increasing conductivity. This is opposite to metals (conductors), where conductivity decreases with temperature.

2. Intrinsic & Extrinsic Semiconductors, Doping, P-Type and N-Type

2.1 Intrinsic Semiconductor

An intrinsic semiconductor is a pure semiconductor material with no impurities added. In its pure form, the electrical properties are determined entirely by its own atomic structure. Silicon (Si) and Germanium (Ge) are the most commonly used intrinsic semiconductors. Both belong to Group IV of the periodic table and have four valence electrons, forming covalent bonds with neighbouring atoms.

At absolute zero (0 K), all covalent bonds are intact and no free carriers are available — the material behaves as an insulator. At room temperature (300 K), thermal energy breaks some covalent bonds, releasing free electrons (negative charge carriers) and creating holes (positive charge carriers). In an intrinsic semiconductor, the number of free electrons always equals the number of holes.

$$n_i = p_i \rightarrow n \times p = n_i^2$$

Law of Mass Action: n = electron concentration, p = hole concentration, ni = intrinsic carrier concentration

Definition: A hole is a vacant position left behind when a covalent bond is broken. It behaves as a positive charge carrier with the same magnitude of charge as an electron ($+1.6 \times 10^{-19}$ C).

Properties of Intrinsic Semiconductor

- Equal numbers of free electrons and holes: n = p = ni
- Very poor conductor at room temperature — used mainly as base material for extrinsic semiconductors
- Conductivity increases with increasing temperature
- Fermi level lies at the middle of the forbidden energy gap
- Not directly suitable for practical electronic devices without doping

2.2 Extrinsic Semiconductor

An extrinsic semiconductor is one in which controlled amounts of specific impurities are added to a pure (intrinsic) semiconductor to drastically alter its electrical properties. This process of adding impurities is called doping, and the impurities added are called dopants. The resulting semiconductor has significantly higher electrical conductivity than the intrinsic material.

2.3 Concept of Doping Concentration

Doping concentration refers to the number of impurity atoms added per unit volume of the semiconductor material. The doping level controls how many additional charge carriers (electrons or holes) are

introduced. Typical doping concentrations range from 10^{13} to 10^{19} atoms per cm^3, compared to the intrinsic carrier concentration of silicon at room temperature of about 1.5×10^{10} per cm^3.

- Light doping (10^{13} to 10^{15} /cm^3): Slightly improved conductivity
- Moderate doping (10^{15} to 10^{17} /cm^3): Used in most general-purpose diodes and transistors
- Heavy doping (10^{17} to 10^{19} /cm^3): Used in tunnel diodes and ohmic contacts

Important Note: Even a small amount of doping (1 impurity atom per 10^7 semiconductor atoms) can increase conductivity by a factor of thousands. This makes doping a very powerful tool for controlling semiconductor behaviour.

2.4 N-Type Semiconductor

Formation

An N-type semiconductor is formed by adding pentavalent impurity atoms (atoms with 5 valence electrons) to a pure semiconductor such as silicon. Commonly used pentavalent dopants include Phosphorus (P), Arsenic (As), and Antimony (Sb). When a pentavalent atom replaces a silicon atom in the crystal lattice, four of its five valence electrons form covalent bonds with the four neighbouring silicon atoms. The fifth electron is not needed for bonding and becomes a free electron with very little energy required to detach it from the donor atom.

Dopant Type: Pentavalent impurities (5 valence electrons): Phosphorus, Arsenic, Antimony — called DONOR atoms because they donate free electrons.

Properties of N-Type Semiconductor

- Majority carriers: Electrons (donated by pentavalent impurity atoms)
- Minority carriers: Holes (thermally generated, in small numbers)
- The material is electrically neutral overall — the extra electrons are balanced by the positive charge of the donor ion cores
- Fermi level shifts closer to the conduction band (higher energy side)
- Conductivity is much higher than the intrinsic semiconductor
- For every donor atom, one extra free electron is added: n ≈ ND (donor concentration)

$$n \approx N_D \quad \text{and} \quad p = n_i^2 / N_D$$

N-type: n = electron density, ND = donor concentration, ni = intrinsic concentration

2.5 P-Type Semiconductor

Formation

A P-type semiconductor is formed by adding trivalent impurity atoms (atoms with 3 valence electrons) to a pure semiconductor. Commonly used trivalent dopants include Boron (B), Aluminium (Al), Gallium (Ga),

and Indium (In). When a trivalent atom replaces a silicon atom, it can form covalent bonds with only three of the four neighbouring silicon atoms because it has only three valence electrons. This leaves one unsatisfied bond — a vacancy called a hole — which can accept an electron from a nearby atom. The trivalent impurity atom is therefore called an acceptor atom.

Dopant Type: Trivalent impurities (3 valence electrons): Boron, Aluminium, Gallium, Indium — called ACCEPTOR atoms because they create holes that accept electrons.

Properties of P-Type Semiconductor

- Majority carriers: Holes (created by trivalent impurity atoms)
- Minority carriers: Electrons (thermally generated, in small numbers)
- The material remains electrically neutral overall
- Fermi level shifts closer to the valence band (lower energy side)
- Conductivity is much higher than intrinsic semiconductor
- For every acceptor atom, one hole is created: p ≈ NA (acceptor concentration)

$$p \approx N_A \quad \text{and} \quad n = n_i^2 / N_A$$

P-type: p = hole density, NA = acceptor concentration

2.6 Comparison: Intrinsic vs N-Type vs P-Type

Property	Intrinsic	N-Type	P-Type
Impurity	None (pure)	Pentavalent (Donor)	Trivalent (Acceptor)
Majority Carrier	Equal e^- and holes	Electrons	Holes
Minority Carrier	None (equal)	Holes	Electrons
Fermi Level	Middle of gap	Near conduction band	Near valence band
Examples of Dopant	—	P, As, Sb	B, Al, Ga, In
Conductivity	Low	Higher (due to e^-)	Higher (due to holes)

3. Formation of P-N Junction Diode and Their Properties

3.1 Formation of P-N Junction

A P-N junction is formed when a P-type semiconductor and an N-type semiconductor are brought into intimate contact — typically by diffusing a P-type dopant into one side of an N-type semiconductor wafer (or vice versa). The point or region where the two types of semiconductor material meet is called the P-N junction.

Depletion Region and Built-in Potential

When the P-N junction is first formed, free electrons from the N-side diffuse across the junction into the P-side, and holes from the P-side diffuse across into the N-side. This process of diffusion is driven by the concentration gradient of carriers. As electrons and holes cross the junction, they recombine with each other near the junction boundary, leaving behind fixed, immobile ionic charges — positive donor ions on the N-side and negative acceptor ions on the P-side.

This region near the junction — depleted of free charge carriers — is called the Depletion Region (also called the Space Charge Region or Depletion Layer). The fixed charges in the depletion region create an electric field directed from N to P, which opposes further diffusion. Eventually, equilibrium is reached and a stable built-in potential (barrier potential) is established across the junction.

Barrier Potential (V_0): ~0.7 V for Silicon, ~0.3 V for Germanium

At room temperature (300 K)

Depletion Region: A region around the P-N junction depleted of free carriers, containing fixed ionized donor (+) and acceptor (-) charges. It acts as a barrier to current flow and gives the junction its rectifying properties.

3.2 Forward Biasing of P-N Junction Diode

When an external voltage is applied with the positive terminal connected to the P-side and the negative terminal to the N-side, the diode is said to be forward biased. The applied voltage opposes the built-in barrier potential, reducing the width of the depletion region. When the applied voltage exceeds the barrier potential (0.7 V for Si, 0.3 V for Ge), the depletion region virtually disappears and a large current flows through the junction — the diode conducts.

- Positive terminal of battery → P-side; Negative terminal → N-side
- Depletion region narrows and eventually disappears
- Large current flows (in milliamps to amps range)
- The diode acts like a closed switch (low resistance path)
- Threshold/Cut-in voltage: 0.7 V (Si), 0.3 V (Ge)

3.3 Reverse Biasing of P-N Junction Diode

When the external voltage is applied with the positive terminal connected to the N-side and the negative terminal to the P-side, the diode is said to be reverse biased. The applied voltage adds to the built-in barrier potential, causing the depletion region to widen further. This blocks majority carrier current flow. Only a tiny leakage current called the Reverse Saturation Current (I_0) flows, due to minority carriers — this is in the range of microamps (μA) or nanoamps (nA).

- Positive terminal of battery → N-side; Negative terminal → P-side
- Depletion region widens — more barrier for carriers
- Only very small reverse saturation current (I_0) flows
- The diode acts like an open switch (very high resistance)

3.4 V-I Characteristics of P-N Junction Diode

The V-I characteristic curve shows the relationship between the voltage applied across the diode and the resulting current. The diode equation (Shockley Equation) mathematically describes this relationship:

$$I = I_0 \left[e^{(V / \eta VT)} - 1 \right]$$

Shockley Diode Equation: I_0 = reverse saturation current, η = ideality factor (1 for Ge, 2 for Si), VT = thermal voltage = kT/q ≈ 26 mV at 300K

Key Points of V-I Characteristics

- In forward bias, current rises exponentially once the cut-in voltage is exceeded
- In reverse bias, a very small and nearly constant reverse saturation current flows
- At a sufficiently large reverse voltage, the diode undergoes Breakdown (Zener or Avalanche), and current increases sharply

3.5 Breakdown Mechanisms

- **Zener Breakdown:** Zener Breakdown
- Occurs in heavily doped diodes at low reverse voltages (< 5 V). The strong electric field at the junction directly pulls electrons from the valence band to the conduction band (band-to-band tunneling). Zener diodes use this controlled breakdown for voltage regulation.
- **Avalanche Breakdown:** Avalanche Breakdown
- Occurs in lightly doped diodes at higher reverse voltages (> 6 V). Minority carriers gain enough energy to ionize atoms by collision, creating more carrier pairs — a multiplicative avalanche process.

3.6 Applications of P-N Junction Diode

- Rectifier: Converts AC to pulsating DC (half-wave and full-wave rectifiers)
- Clipping and Clamping Circuits: Used in wave-shaping applications
- Zener Diode: Voltage regulation, voltage reference circuits
- LED (Light Emitting Diode): Converts electrical energy to light — displays, indicators

- Photodiode: Converts light energy to electrical current — light sensing, optical communication
- Solar Cell: Converts sunlight into electrical energy
- Varactor Diode: Variable capacitance — used in tuning circuits, voltage-controlled oscillators

Parameter	Forward Bias	Reverse Bias
Connection	+ve → P-side, -ve → N-side	+ve → N-side, -ve → P-side
Depletion Region	Narrows / disappears	Widens
Current	Large (mA to A)	Very small (μA or nA)
Resistance	Very low	Very high
Switch Equivalent	Closed switch	Open switch

4. PNP and NPN Transistors — Concept and Applications

4.1 Introduction to Transistor

A transistor (Transfer Resistor) is a three-terminal, two-junction semiconductor device that can amplify electrical signals or act as a switch. It is the fundamental building block of modern electronic circuits. The transistor was invented in 1947 at Bell Laboratories by John Bardeen, Walter Brattain, and William Shockley.

A Bipolar Junction Transistor (BJT) is formed by sandwiching one type of semiconductor between two layers of the opposite type. This creates two P-N junctions. Based on the arrangement, transistors are classified as NPN and PNP types.

4.2 NPN Transistor

Construction

An NPN transistor consists of a thin layer of P-type semiconductor (called the Base) sandwiched between two N-type semiconductor regions. The three terminals are: Emitter (E), Base (B), and Collector (C).

- Emitter (E): Heavily doped N-type region — emits majority carriers (electrons) into the base
- Base (B): Very thin, lightly doped P-type region — controls the flow of carriers
- Collector (C): Moderately doped N-type region — collects carriers coming from the emitter

Working Principle of NPN Transistor (in Active Mode)

In the active region, the emitter-base (EB) junction is forward biased and the collector-base (CB) junction is reverse biased. Forward biasing of the EB junction causes a large number of electrons to flow from the emitter into the thin base region. Since the base is very thin and lightly doped, most of these electrons (about 95-99%) diffuse across the base without recombining and are swept into the collector by the reverse-biased CB junction's electric field. Only a small fraction (1-5%) of electrons recombine with holes in the base, forming the small base current IB.

$$I_E = I_B + I_C \quad \text{and} \quad I_C = \beta \times I_B$$

Transistor current relations: β = DC current gain (hFE), typically 20 to 500

Current Direction in NPN: Conventional current flows: Collector → Emitter (externally). Electron flow: Emitter → Collector (internally through the device).

4.3 PNP Transistor

Construction

A PNP transistor consists of a thin N-type semiconductor layer (Base) sandwiched between two P-type semiconductor regions (Emitter and Collector).

- Emitter (E): Heavily doped P-type region — emits holes into the base
- Base (B): Very thin, lightly doped N-type region — controls carrier flow
- Collector (C): Moderately doped P-type region — collects holes from the emitter

Working Principle of PNP Transistor

In the active region of a PNP transistor, the EB junction is forward biased (emitter positive w.r.t. base) and the CB junction is reverse biased. The forward-biased EB junction causes holes to be injected from the emitter into the base. As with NPN, the base is thin and lightly doped, so most holes diffuse through the base and are swept into the collector region. The operation is analogous to NPN but with holes as the majority charge carriers instead of electrons.

Current Direction in PNP: Conventional current flows: Emitter → Collector (externally). The emitter current IE = IB + IC, and IC = β × IB (same relations hold).

4.4 Transistor Configurations

A transistor can be connected in three different configurations in a circuit, depending on which terminal is common to both input and output:

Configuration	Input	Output	Current Gain	Voltage Gain	Phase Shift
Common Emitter (CE)	Base-Emitter	Collector-Emitter	β = IC/IB (high)	High	180°
Common Base (CB)	Emitter-Base	Collector-Base	α = IC/IE (<1)	High	0°
Common Collector (CC)	Base-Collector	Emitter-Collector	γ = IE/IB (high)	< 1	0°

Most Common: Common Emitter (CE) configuration is the most widely used because it provides both current gain and voltage gain, making it ideal for amplifier circuits.

4.5 Comparison: NPN vs PNP Transistor

Feature	NPN Transistor	PNP Transistor
Majority carriers	Electrons	Holes
Emitter material	N-type (heavily doped)	P-type (heavily doped)
Base material	P-type (thin, lightly doped)	N-type (thin, lightly doped)
Collector material	N-type	P-type
Supply Polarity	+VCC at Collector	-VCC at Collector
Speed	Faster (electrons more mobile)	Slower (holes less mobile)

Symbol Arrow	Arrow away from base (outward)	Arrow toward base (inward)
Common Use	Most common in digital circuits	Complementary pair with NPN

4.6 Applications of Transistors

- Amplifier: Amplifies weak signals in audio, radio, and instrumentation systems (CE configuration most common)
- Switch: Used as electronic switch in digital logic circuits, relays, LED drivers, motor control
- Oscillator: Generates AC signals of required frequency in radio transmitters and clock circuits
- Signal Modulation and Demodulation: Used in communication circuits
- Voltage Regulator: In linear voltage regulator circuits
- Darlington Pair: Two transistors cascaded for very high current gain
- Logic Gates: The building blocks of all digital logic (AND, OR, NOT gates)

5. FET, MOSFET & CMOS — Concept and Applications

5.1 Field Effect Transistor (FET)

Introduction

A Field Effect Transistor (FET) is a three-terminal semiconductor device in which the current through the device is controlled by an electric field (voltage), rather than by a base current as in a BJT. This makes the FET a voltage-controlled device, whereas the BJT is a current-controlled device. FETs have extremely high input impedance (typically in the order of megaohms to gigaohms), making them ideal for amplifiers in high-impedance measurement circuits.

Key Difference: BJT = Current-Controlled Device (input current controls output current). FET = Voltage-Controlled Device (input voltage controls output current). FET has much higher input impedance than BJT.

Terminals of FET

- Gate (G): The control terminal — analogous to the Base of a BJT. Voltage applied here controls the channel.
- Drain (D): The terminal through which majority carriers leave the channel — analogous to Collector of BJT.
- Source (S): The terminal through which majority carriers enter the channel — analogous to Emitter of BJT.

Types of FET

- Junction FET (JFET): Uses a reverse-biased P-N junction to control the channel width. Two subtypes: N-channel JFET and P-channel JFET.
- Metal Oxide Semiconductor FET (MOSFET): Uses an insulated gate (metal-oxide-semiconductor structure) to control the channel. The most important and widely used FET type.

5.2 JFET — Junction Field Effect Transistor

Construction and Working

In an N-channel JFET, a bar of N-type semiconductor forms the main current-carrying channel between the Source and Drain terminals. P-type regions are diffused on both sides of the N-channel to form the Gate. A reverse bias is applied between the Gate and Source (VGS < 0 for N-channel). The reverse-biased P-N junctions create depletion regions that extend into the N-channel. By varying VGS, the width of the depletion region is varied, which effectively controls the cross-sectional area of the channel and hence the drain current (ID).

- When VGS = 0: Channel is widest, maximum drain current (IDSS) flows
- When VGS becomes more negative: Depletion regions expand, channel narrows, ID decreases
- When VGS = VP (Pinch-off voltage): Channel is completely pinched off, ID ≈ 0

$$ID = IDSS \times (1 - VGS/VP)^2$$

Shockley's Equation for JFET (in saturation region)

5.3 MOSFET — Metal Oxide Semiconductor Field Effect Transistor

Introduction

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is the most important and widely used transistor in modern electronics. Unlike the JFET, the gate terminal of a MOSFET is electrically insulated from the semiconductor channel by a thin layer of silicon dioxide (SiO_2), which acts as a dielectric. This gives the MOSFET an extremely high input impedance (practically infinite) and allows the gate voltage to be positive or negative without any gate current flowing.

Construction of MOSFET

A MOSFET consists of a P-type (or N-type) semiconductor substrate on which two heavily doped N-type (or P-type) regions — called Source and Drain — are formed by diffusion or ion implantation. The region between the Source and Drain on the substrate surface is called the channel region. A thin layer of silicon dioxide (SiO_2) is grown over the channel region, and on top of this oxide layer, a metal or polysilicon gate electrode is deposited. The SiO_2 layer acts as an insulator between the gate and the channel, which is why MOSFETs are also called Insulated Gate FETs (IGFETs).

Types of MOSFET

- **Enhancement Mode:** Enhancement Mode MOSFET (E-MOSFET): No physical channel exists between source and drain at zero gate voltage. A channel is induced (enhanced) by applying a positive gate voltage (for N-channel). This is the most commonly used type in digital circuits.

- **Depletion Mode:** Depletion Mode MOSFET (D-MOSFET): A physical channel exists between source and drain at zero gate voltage (the device is normally ON). A negative gate voltage depletes the channel carriers, reducing or cutting off the current.

Working of N-Channel Enhancement MOSFET

With no gate voltage (VGS = 0), there is no channel between drain and source and no current flows. When a positive voltage is applied to the gate (VGS > 0), the electric field penetrates the SiO_2 layer and attracts free electrons from the P-type substrate to the surface beneath the oxide. When VGS exceeds a threshold voltage (VT), a thin N-type channel (inversion layer) is formed between the source and drain, allowing current to flow from drain to source. The greater the VGS, the wider and more conductive the channel becomes.

$$ID = K\ (VGS - VT)^2 \quad (for\ VDS > VGS - VT)$$

MOSFET current equation in saturation: K = process transconductance, VT = threshold voltage

Feature	BJT	JFET	MOSFET

Type	Current-controlled	Voltage-controlled	Voltage-controlled
Input Impedance	Low (~kΩ)	High (~MΩ)	Very High (~GΩ)
Gate Current	IB flows	Negligible	Practically zero
Control Mechanism	Base current	Reverse-biased junction	Electric field (oxide gate)
Noise	Moderate	Low	Very low
Operating Mode	Active, Saturation, Cutoff	Pinch-off, Saturation	Enhancement, Depletion
Digital Use	Less common (power)	Less common	Dominant (VLSI, CMOS)

5.4 CMOS — Complementary Metal Oxide Semiconductor

Introduction

CMOS (Complementary Metal Oxide Semiconductor) is a technology that uses complementary pairs of P-channel MOSFET (PMOS) and N-channel MOSFET (NMOS) to implement digital logic circuits. The term 'complementary' refers to the use of both PMOS and NMOS transistors working together in a complementary manner. CMOS is the dominant technology used in microprocessors, memory chips, and virtually all modern digital integrated circuits.

CMOS Inverter — Basic Building Block

The basic CMOS circuit is an inverter (NOT gate). It consists of one PMOS transistor connected between the supply voltage (VDD) and the output, and one NMOS transistor connected between the output and ground (VSS). The gates of both transistors are connected together as the input.

- When input is HIGH (logic 1): NMOS turns ON, PMOS turns OFF → Output is LOW (logic 0). The output is pulled to ground through the NMOS.
- When input is LOW (logic 0): PMOS turns ON, NMOS turns OFF → Output is HIGH (logic 1). The output is pulled to VDD through the PMOS.

Key CMOS Principle: In a CMOS circuit, either PMOS or NMOS is ON at any time — never both simultaneously (in steady state). This means negligible static power dissipation — the most important advantage of CMOS.

Advantages of CMOS Technology

- Extremely low static power dissipation — power is consumed only during switching transitions
- High noise immunity — large noise margins due to full-swing output (0 to VDD)
- Very high integration density — billions of transistors on a single chip
- Scalable — performance improves as transistor size is reduced (Moore's Law)
- Compatible with both analog and digital design on the same chip
- Wide operating voltage range and temperature tolerance

Disadvantages of CMOS

- Dynamic power dissipation increases with switching frequency
- Complex fabrication process compared to NMOS-only technology
- Susceptible to latch-up in bulk CMOS due to parasitic BJT structures

5.5 Applications

JFET Applications

- High-impedance amplifier stages (microphone preamplifiers, oscilloscope front-ends)
- Voltage-controlled resistors in AGC (Automatic Gain Control) circuits
- Low-noise amplifiers in radio receivers
- Source followers (high-impedance buffers)

MOSFET Applications

- Power MOSFETs: High-current switching in power supplies, motor drives, inverters
- RF MOSFETs: In mobile phone power amplifiers
- Digital logic: All VLSI logic circuits use MOSFET
- Memory cells: DRAM (Dynamic RAM) uses a MOSFET + capacitor per bit
- Analog circuits: Op-amps, sample-and-hold circuits

CMOS Applications

- Microprocessors and microcontrollers (Intel, AMD, ARM — all use CMOS)
- Static RAM (SRAM) and Flash memory (NAND, NOR Flash)
- Image sensors — CMOS image sensors (in smartphones, cameras)
- Digital logic gates, flip-flops, counters, multiplexers
- Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC)
- Wireless communication chips, Bluetooth, Wi-Fi, 5G modems
- Wearable electronics and IoT devices — where ultra-low power is critical

5.6 Quick Reference: FET, MOSFET & CMOS Summary

Device	Type	Key Feature	Main Application
N-Channel JFET	Depletion (normally ON)	Voltage-controlled, high Zi	Low-noise amplifiers, VCR
P-Channel JFET	Depletion (normally ON)	Complementary to N-JFET	Analog switches, amplifiers
E-MOSFET (NMOS)	Enhancement (normally OFF)	Insulated gate, very high Zi	Digital logic, VLSI
E-MOSFET (PMOS)	Enhancement (normally OFF)	Complementary to NMOS	CMOS circuits, pull-up

D-MOSFET	Depletion (normally ON)	Can work ±VGS	Analog switches
Power MOSFET	Enhancement, large area	High current, low RDS(on)	Motor drives, power supplies
CMOS Logic	NMOS + PMOS pair	Near-zero static power	All digital ICs, processors

End of Chapter: Overview of Basic Semiconductor Devices
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