
Electronics Devices & Circuits

Chapter 5

OPERATIONAL AMPLIFIER

Detailed Study Notes for Engineering Students

Differential Amplifier • Op-Amp Characteristics • Op-Amp Applications

Includes diagrams, worked examples, 15 MCQs with answer key and 10 broad questions

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Chapter 5: Operational Amplifier

An **operational amplifier (op-amp)** is a high-gain, direct-coupled (DC) amplifier with a differential input and (usually) a single-ended output. It was originally developed to perform mathematical *operations* such as addition, subtraction, integration and differentiation in analog computers, which is how it got its name. Today the op-amp is available as a cheap integrated circuit (IC) such as the **IC 741**, and it is the basic building block of amplifiers, filters, oscillators, signal conditioners, comparators, converters and many other analog systems.

This chapter first studies the **differential amplifier** (the input stage of every op-amp), then the **terms and parameters** used to describe an op-amp, and finally the most important **op-amp circuits**.

Table 5.1: Scope of the chapter

Section	Topics covered
5.1	Circuit operation of differential amplifier
5.2	Introduction to op-amp; inverting and non-inverting modes and gain calculation; CMRR; bias current; offset voltage and current; slew rate; open-loop and closed-loop gain; input and output impedance; frequency response; virtual ground
5.3	Applications of op-amp: adder, subtractor, voltage follower, integrator, differentiator, comparator, Schmitt trigger
End	Chapter summary (key formulas), 15 MCQs with answer key, 10 broad questions

5.1 Circuit Operation of Differential Amplifier

A **differential amplifier** (diff-amp) amplifies the **difference** between two input signals and rejects (suppresses) the part of the signal that is **common** to both inputs. Noise, hum, interference and temperature drift usually appear equally on both input lines, so a diff-amp automatically removes most of the unwanted signal while keeping the wanted one. For this reason the diff-amp is used as the first stage of every op-amp.

5.1.1 Advantages of a differential amplifier

- It is **direct coupled**, so it amplifies DC and very low-frequency signals (no coupling or bypass capacitors are needed). This makes it ideal for IC fabrication, where large capacitors are impractical.
- It has a **high common-mode rejection ratio (CMRR)**, so noise and drift are strongly reduced.
- Two matched transistors on the same chip track each other with temperature, which gives **low drift**.
- It can accept two inputs (**dual-input**) or one input (**single-input**) and can give a balanced or an unbalanced output.

5.1.2 Basic circuit and construction

The basic BJT differential amplifier is shown below. It consists of two **identical (matched) transistors** Q1 and Q2. The emitters are joined together and connected to a common emitter resistor R_E , which returns to the negative supply $-V_{EE}$. Each collector has its own collector resistor R_C connected to $+V_{CC}$. The signals v_1 and v_2 are applied at the two bases, and the outputs v_{o1} and v_{o2} are taken from the two collectors.

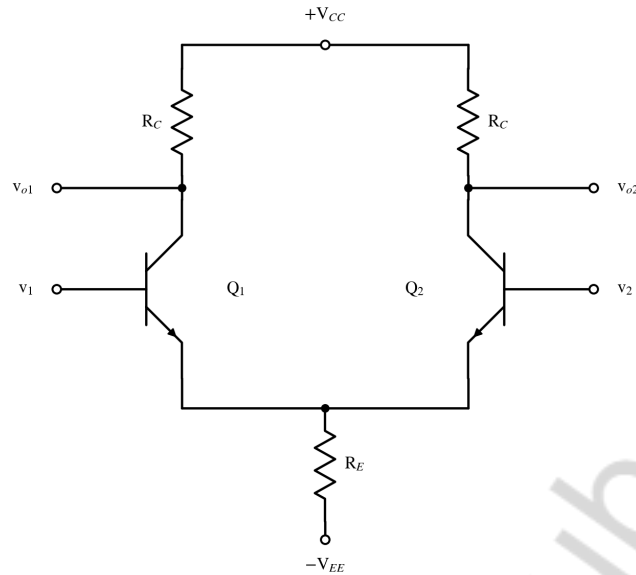


Fig. 5.1: Basic differential amplifier using two matched BJTs

- **Two supplies** ($+V_{CC}$ and $-V_{EE}$) are used so that the bases can be kept near 0 V (ground) without any biasing resistor.
- **Symmetry:** $Q1 = Q2$ (same β , V_{BE}), and the two R_C resistors are equal. The circuit is perfectly symmetrical about the vertical axis.
- **Balanced output** means the output is taken *between* the two collectors, $v_o = v_{o1} - v_{o2}$.
- **Unbalanced (single-ended) output** means the output is taken from one collector with respect to ground.

5.1.3 Differential-mode and common-mode signals

Any pair of input voltages v_1 and v_2 can be split into two parts:

Table 5.2: Differential and common-mode signals

Quantity	Definition	Meaning
Differential input v_d	$v_d = v_1 - v_2$	The wanted signal that the amplifier should amplify
Common-mode input v_c	$v_c = (v_1 + v_2) / 2$	The part that is the same at both inputs (noise, hum) and should be rejected
Reconstruction	$v_1 = v_c + v_d/2$; $v_2 = v_c - v_d/2$	Any two inputs are a mixture of these two

$$\text{Output: } v_o = A_d v_d + A_c v_c$$

Here A_d is the **differential gain** (should be large) and A_c is the **common-mode gain** (should be very small). Their ratio is the CMRR (Section 5.1.7).

5.1.4 DC (bias) analysis

For DC analysis both inputs are grounded ($v_1 = v_2 = 0$). Neglecting the small base currents, the base voltage is 0 V, so the emitter voltage is $V_E = -V_{BE}$. Applying KVL through R_E gives the total emitter current:

$$I_{E(\text{total})} = (V_{EE} - V_{BE}) / R_E$$

$$I_{E1} = I_{E2} = I_E = I_{E(\text{total})} / 2 \approx I_C$$

$$V_C = V_{CC} - I_C R_C ; \quad V_{CE} = V_C - V_E = V_{CC} - I_C R_C + V_{BE}$$

The ac emitter resistance of each transistor depends on its own emitter current:

$$r_e = V_T / I_E \approx 26 \text{ mV} / I_E \quad (V_T = \text{thermal voltage} \approx 26 \text{ mV at room temperature})$$

5.1.5 Circuit operation (working)

The working of the diff-amp is understood by considering what happens to the two transistors for different input conditions. Because of the common emitter resistor, the two transistors *share* a nearly fixed total emitter current.

Table 5.3: Operation of the differential amplifier

Input condition	What happens inside the circuit	Result at output
Case 1: $v_1 = v_2$ (pure common-mode)	Both transistors conduct equally more (or less). The emitter voltage follows the input, so the current through R_E changes and R_E produces strong negative feedback , which opposes the change.	v_{o1} and v_{o2} change by the same small amount. Balanced output $v_{o1} - v_{o2} \approx 0 \rightarrow$ common signal is rejected .
Case 2: $v_1 > v_2$ (differential)	Q1 conducts more; Q2 conducts less. Since the total emitter current is almost constant, the increase in I_{C1} equals the decrease in I_{C2} .	Drop across R_{C1} increases, so v_{o1} falls ; v_{o2} rises . A large difference output appears.
Case 3: $v_1 = -v_2$ (pure differential)	Current increase in one transistor is exactly the current decrease in the other, so the emitter point stays at a constant (ac ground) potential. R_E has no effect on the signal.	Maximum gain, determined only by R_C and r_e .
Case 4: single input (one input grounded)	The signal at Q1 base also changes the common emitter voltage, which drives Q2 as a common-base stage. The action is the same as with a differential input $v_d = v_1$.	Still amplified; the output depends on the difference $v_1 - 0$.

Note: The above small-signal action is linear only for small differential inputs (about a few tens of millivolts). For larger v_d , one transistor cuts off and the other carries the entire emitter current, so the output saturates.

5.1.6 Differential gain, input resistance and output resistance

Using the ac equivalent circuit (each transistor replaced by its r_e model) the following results are obtained. The four possible configurations differ in the way input is applied (one or two inputs) and in the way output is taken (balanced or unbalanced).

Table 5.4: Four configurations of a differential amplifier

Configuration	Input applied	Output taken	Differential gain A_d	Input resistance R_{id}	Output resistance R_o
1. Dual-input, balanced-output	v_1 and v_2	$v_{o1} - v_{o2}$	R_C / r_e	$2\beta r_e$	$2 R_C$
2. Dual-input, unbalanced-output	v_1 and v_2	v_{o1} (or v_{o2}) to ground	$R_C / 2r_e$	$2\beta r_e$	R_C
3. Single-input, balanced-output	v_1 only ($v_2 = 0$)	$v_{o1} - v_{o2}$	R_C / r_e	$2\beta r_e$	$2 R_C$
4. Single-input, unbalanced-output	v_1 only ($v_2 = 0$)	v_{o1} (or v_{o2}) to ground	$R_C / 2r_e$	$2\beta r_e$	R_C

- The gain depends only on **how the output is taken**: balanced output gives R_C/r_e , unbalanced output gives half of it. Whether one or two inputs are used does not change A_d .
- Balanced output gives **twice** the gain of unbalanced output because the output is the difference of two collector signals that are 180° out of phase.
- In an unbalanced (single-ended) output, v_{o1} is **inverted** with respect to v_1 , and v_{o2} is **in phase** with v_1 .

Common-mode gain. For a common-mode input, both emitter currents flow through R_E , so each half of the circuit sees an effective emitter resistance of $2R_E$. For single-ended output:

$$A_c = -R_C / (2R_E + r_e) \approx -R_C / (2R_E)$$

For a perfectly matched circuit with balanced output, $A_c = 0$ because the two collector voltages change equally and cancel in the difference. In practice a small A_c remains due to mismatch.

5.1.7 Common-mode rejection ratio (CMRR) of the diff-amp

$$\text{CMRR} = |A_d / A_c| \quad \text{CMRR (dB)} = 20 \log_{10} |A_d / A_c|$$

For single-ended output: $\text{CMRR} = [R_C / 2r_e] / [R_C / (2R_E + r_e)] \approx R_E / r_e$. So the CMRR can be increased by **making R_E larger** or r_e smaller. A larger R_E , however, needs a larger V_{EE} to keep the same bias current, which is wasteful. The practical solution is described next.

5.1.8 Constant current source in place of R_E

A transistor biased as a **constant current source** (Q3 in the IC) can replace R_E . It sets the same total emitter current, but its *ac (dynamic) resistance* is very high (hundreds of $k\Omega$ to $M\Omega$), while only a small DC voltage is dropped across it. As R_E is effectively very large, A_c becomes very small and the CMRR rises to 80–100 dB. This is exactly how the input stage of the IC 741 is built.

Example 5.1

Given: $V_{CC} = V_{EE} = 12 \text{ V}$, $R_C = 5 \text{ k}\Omega$, $R_E = 10 \text{ k}\Omega$, $V_{BE} = 0.7 \text{ V}$, $\beta = 100$. Find the DC currents, differential gain (balanced and single-ended outputs), common-mode gain (single-ended) and CMRR.

Step 1 (bias): $I_{E(\text{total})} = (12 - 0.7) / 10 \text{ k}\Omega = 1.13 \text{ mA}$, so $I_E = I_C \approx 0.565 \text{ mA}$ per transistor.

Step 2: $V_C = 12 - (0.565 \text{ mA})(5 \text{ k}\Omega) = 12 - 2.83 = 9.17 \text{ V}$.

Step 3: $r_e = 26 \text{ mV} / 0.565 \text{ mA} = 46 \Omega$.

Step 4: A_d (balanced) $= R_C / r_e = 5000 / 46 \approx 108.7$; A_d (single-ended) $= 108.7 / 2 \approx 54.3$.

Step 5: A_c (single-ended) $= R_C / (2R_E + r_e) = 5000 / 20046 \approx 0.25$.

Step 6: $\text{CMRR} = 54.3 / 0.25 \approx 218$, i.e. $20 \log_{10}(218) \approx 46.8 \text{ dB}$. Input resistance $R_{id} = 2\beta r_e = 2(100)(46) = 9.2 \text{ k}\Omega$.

5.2 Introduction to Operational Amplifier

5.2.1 What is an op-amp?

An op-amp is a **multistage, direct-coupled, high-gain voltage amplifier** with two inputs and one output. Its output is proportional to the *difference* between the voltages at the two inputs:

$$v_o = A_{OL} (v_+ - v_-) = A_{OL} v_d$$

- **Inverting input (-):** a signal applied here appears at the output with a **180° phase shift**.
- **Non-inverting input (+):** a signal applied here appears at the output **in phase**.
- **Output:** single-ended, referred to ground. It cannot exceed about $\pm V_{sat}$, which is 1–2 V less than the supply voltage.
- **Supplies:** normally dual supply ± 5 V to ± 15 V (e.g. +15 V and -15 V). Note that the IC has no ground pin; ground is only the common reference point of the external circuit.

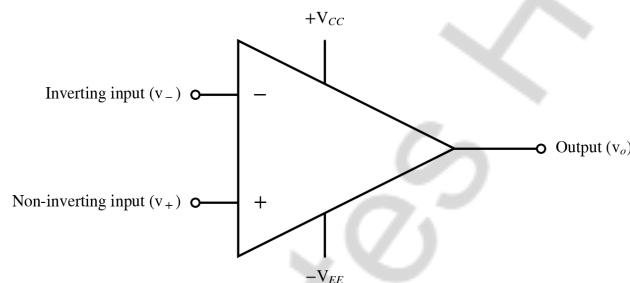


Fig. 5.2: Circuit symbol of an op-amp with supply connections

Internal block diagram

Inside the IC there are four main blocks connected in cascade (direct coupling):

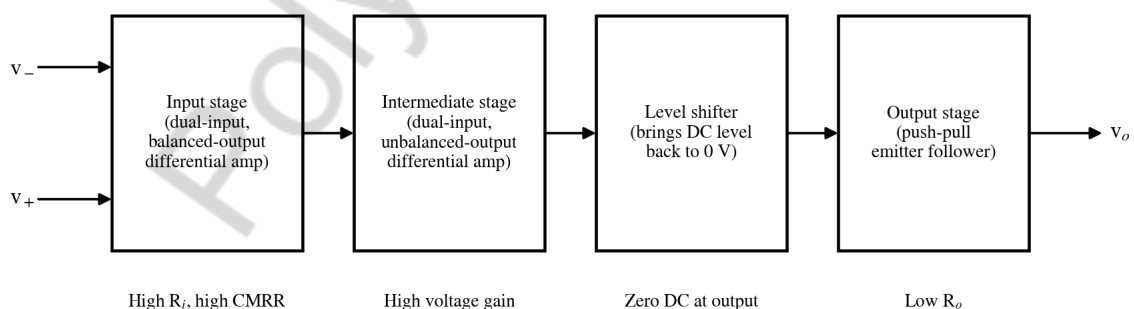
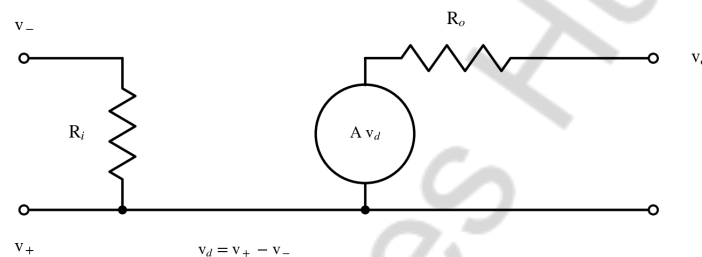


Fig. 5.3: Block diagram of an operational amplifier

Table 5.5: Function of each stage inside an op-amp

Stage	Function
Input stage (differential amplifier)	Dual-input balanced-output diff-amp. Gives high input resistance, high CMRR and low noise. This is the stage studied in Section 5.1.
Intermediate stage	Another diff-amp (with dual-input, unbalanced output) that provides most of the voltage gain. Several stages may be used, with active loads.
Level shifter	Because of direct coupling, the DC level rises stage by stage. The level shifter (emitter follower with current source) brings the DC level back so that the output is 0 V when both inputs are 0 V.
Output stage	Complementary push-pull emitter follower (class AB). Gives low output resistance, large current drive, and short-circuit protection.

5.2.2 Equivalent circuit, ideal and practical characteristics

*Fig. 5.4: Equivalent circuit of an op-amp*

The input terminals see an **input resistance** R_i . The internal controlled source produces $A_{OL} v_d$, and the **output resistance** R_o is in series with the output terminal.

Table 5.6: Ideal and practical op-amp parameters

Parameter	Ideal op-amp	Practical IC 741 (typical)
Open-loop voltage gain A_{OL}	∞	2×10^5 (106 dB)
Input resistance R_i	∞	2 M Ω
Output resistance R_o	0	75 Ω
Bandwidth	∞	1 MHz (unity-gain bandwidth)
CMRR	∞	90 dB
Slew rate	∞	0.5 V/ μ s
Input offset voltage V_{IO}	0	2 mV (max 6 mV)
Input bias current I_B	0	80 nA (max 500 nA)
Input offset current I_{IO}	0	20 nA (max 200 nA)
Supply voltage range	—	± 5 V to ± 18 V

Pin configuration of IC 741

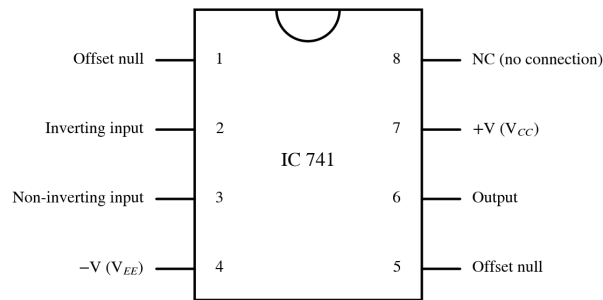


Fig. 5.5: Pin diagram of IC 741 (8-pin DIP, top view)

Pins 1 and 5 are used to connect a potentiometer for **offset nulling**. Pins 2 and 3 are the inverting and non-inverting inputs, pin 6 is the output, pins 7 and 4 receive the positive and negative supplies, and pin 8 is not connected.

5.2.3 Virtual ground and virtual short

The op-amp is almost always used with **negative feedback**, meaning a part of the output is fed back to the inverting input. With feedback, the output stays within the linear range, so the voltage difference at the inputs must be very small:

$$v_d = v_o / A_{OL} \approx 0 \quad (\text{since } A_{OL} \text{ is very large, e.g. } 13 \text{ V} / 200000 = 65 \mu\text{V})$$

This leads to two **golden rules** used to analyse every ideal op-amp circuit with negative feedback:

- **Rule 1 (virtual short):** $v_+ = v_-$. The two input terminals are at the same potential.
- **Rule 2:** The current entering either input terminal is zero (input resistance ∞): $i_+ = i_- = 0$.

Virtual ground: If the non-inverting terminal is connected to ground ($v_+ = 0 \text{ V}$), then by Rule 1 the inverting terminal is also at 0 V, even though it is *not* physically connected to ground. A point that is at ground potential but cannot sink current is called a **virtual ground**. Current coming through the input resistor cannot flow into the op-amp (Rule 2), so it must flow entirely through the feedback resistor.

5.2.4 Inverting mode and gain calculation

In the inverting amplifier the input signal is applied to the inverting terminal through R_1 . The non-inverting terminal is grounded and feedback resistor R_f connects the output to the inverting terminal.

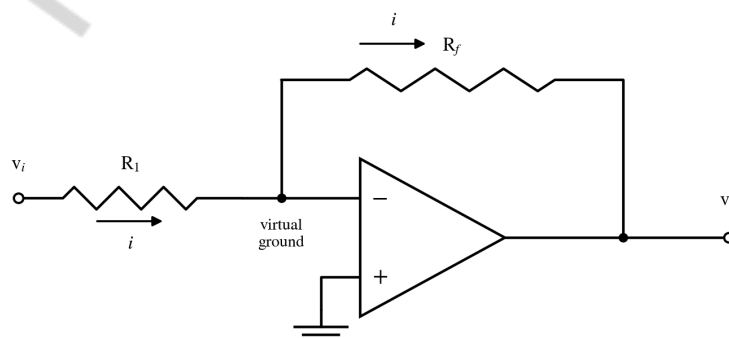


Fig. 5.6: Inverting amplifier

Derivation. Node A (inverting input) is a virtual ground, so $v_- = 0$. Current through R_1 :

$$i = (v_i - 0) / R_1$$

No current enters the op-amp, so the same current flows through R_f (from the virtual ground towards the output):

$$v_o = 0 - i R_f = - (R_f / R_1) v_i$$

Closed-loop gain: $A_{CL} = v_o / v_i = -R_f / R_1$

Input resistance: $R_{in} = R_1$ **Output resistance:** $R_{out} \approx 0$ (very small)

- The negative sign shows a **180° phase shift**: the output is an inverted, amplified (or attenuated) copy of the input.
- The gain magnitude can be set to any value (even less than 1) simply by choosing R_f/R_1 . Gain accuracy depends only on resistor accuracy, not on the op-amp.
- R_{in} is limited to R_1 , so R_1 must be large if a high input resistance is required (but then R_f becomes huge for large gain).
- **Exact gain with finite A_{OL} :** $A_{CL} = -(R_f/R_1) / [1 + (1 + R_f/R_1)/A_{OL}]$, which tends to $-R_f/R_1$ when A_{OL} is very large.

Example 5.2

Given: $R_1 = 10 \text{ k}\Omega$, $R_f = 100 \text{ k}\Omega$, $v_i = 0.5 \text{ V (DC)}$. Find A_{CL} and v_o .

$A_{CL} = -100\text{k}/10\text{k} = -10$. $v_o = (-10)(0.5) = -5 \text{ V}$. For a 1 V peak sine input the output would be a 10 V peak sine wave shifted by 180°, provided $V_{sat} > 10 \text{ V}$.

5.2.5 Non-inverting mode and gain calculation

Here the input signal is applied directly to the non-inverting terminal. The feedback network R_f and R_1 forms a voltage divider connected to the inverting terminal.

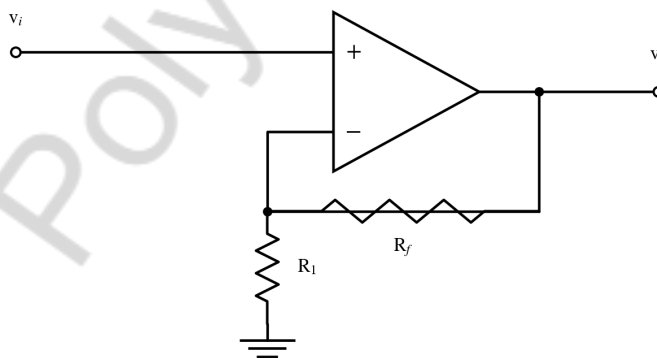


Fig. 5.7: Non-inverting amplifier

Derivation. By the virtual short rule, $v_- = v_+ = v_i$. The voltage at the inverting terminal is the divided output:

$$v_- = v_o \cdot R_1 / (R_1 + R_f) = v_i$$

$$v_o = (1 + R_f / R_1) v_i$$

Closed-loop gain: $A_{CL} = 1 + R_f / R_1$ (always ≥ 1 , positive)

Input resistance: $R_{in} = \text{very high } (R_1(1 + A_{OL} B))$, several hundred M Ω or more) **Output resistance:** very low

Here $B = R_1 / (R_1 + R_f)$ is the feedback factor and the exact gain is $A_{CL} = A_{OL} / (1 + A_{OL} B) \approx 1/B$.

Example 5.3

Given: $R_1 = 1 \text{ k}\Omega$, $R_f = 9 \text{ k}\Omega$, $v_i = 0.4 \text{ V}$. Find the gain and output.

$A_{CL} = 1 + 9\text{k}/1\text{k} = 10$. $v_o = 10 \times 0.4 = 4 \text{ V}$ (in phase with the input).

Table 5.7: Comparison: inverting and non-inverting amplifier

Feature	Inverting amplifier	Non-inverting amplifier
Input applied to	Inverting (–) terminal through R_1	Non-inverting (+) terminal directly
Gain	$-R_f / R_1$	$1 + R_f / R_1$
Phase of output	180° (inverted)	0° (in phase)
Minimum gain magnitude	Can be less than 1	Cannot be less than 1
Input resistance	R_1 (moderate)	Very high
Inverting input node	Virtual ground	At the input voltage (virtual short)
Common-mode voltage on inputs	None (non-inverting at ground)	Equal to v_i ; CMRR matters

5.2.6 Common-mode rejection ratio (CMRR)

An ideal op-amp responds only to the difference v_d . A real op-amp also gives a small output for the common-mode signal v_c . The output of a real op-amp is:

$$v_o = A_d v_d + A_c v_c$$

CMRR = $|A_d / A_c|$ **CMRR (dB)** = $20 \log_{10} |A_d / A_c|$

Ideal CMRR = ∞ . IC 741: typically 90 dB (about 31,600). A higher CMRR means better rejection of noise common to both inputs.

Significance. Noise picked up in long cables, 50 Hz mains hum and thermal drift appear equally on both inputs. A high CMRR ensures this unwanted signal is suppressed, while the small difference signal (for example from a sensor or bridge) is amplified. The CMRR decreases at higher frequencies.

Example 5.4

Given: $A_d = 2 \times 10^5$ and CMRR = 90 dB. Find A_c .

CMRR = $\text{antilog}(90/20) = 10^{4.5} \approx 31,623$. $A_c = A_d / \text{CMRR} = 200000 / 31623 \approx 6.3$. So a 1 mV common-mode noise gives only about 6.3 mV at the output, compared with a gain of 200,000 for the useful difference signal.

5.2.7 Input bias current and input offset current

The input stage of a bipolar op-amp consists of transistors that need small base currents to operate. These currents flow into the two input terminals.

Table 5.8: Bias and offset currents

Term	Definition	Formula	IC 741 value
Input bias current I_B	Average of the two DC currents drawn by the input terminals	$I_B = (I_{B1} + I_{B2}) / 2$	80 nA typical
Input offset current I_{IO}	Difference between the two input bias currents (due to mismatch of the transistors)	$I_{IO} = I_{B1} - I_{B2} $	20 nA typical

- **Effect:** The bias currents flow through the source and feedback resistors and develop unwanted DC voltages, giving a DC error (offset) at the output even when $v_i = 0$.
- **Compensation:** For an inverting amplifier, a compensating resistor $R_{comp} = R_1 \parallel R_f = R_1 R_f / (R_1 + R_f)$ is connected in series with the non-inverting input. The same voltage drop then appears on both inputs and the effect of I_B cancels.
- After compensation only the offset current remains, giving a worst-case output error of about $I_{IO} R_f$.
- Op-amps with FET or MOSFET input stages (e.g. TL081, CA3140) have bias currents in the pA range.

5.2.8 Input offset voltage

In an ideal op-amp the output is exactly zero when both inputs are zero. In a real op-amp, small mismatches in the input transistors cause a non-zero output. **Input offset voltage V_{IO}** is the small DC voltage that must be applied between the two input terminals to make the output voltage exactly zero. For the 741, V_{IO} is typically 2 mV (maximum 6 mV).

The offset is amplified by the noise gain $(1 + R_f/R_1)$, in both inverting and non-inverting mode, and appears at the output:

$$\text{Output offset due to } V_{IO} = \pm V_{IO} (1 + R_f / R_1)$$

$$\text{Total worst-case output offset} \approx V_{IO} (1 + R_f/R_1) + I_{IO} R_f \quad (\text{with compensation resistor used})$$

- **Offset nulling:** A 10 k Ω potentiometer is connected between the offset-null pins 1 and 5 of IC 741, with its wiper connected to the negative supply (pin 4). With $v_i = 0$, the potentiometer is adjusted until $v_o = 0$.
- V_{IO} and I_{IO} also drift with temperature and time, so nulling is not permanent for precision work.

Example 5.5

Given: $V_{IO} = 2$ mV, $R_1 = 1$ k Ω , $R_f = 100$ k Ω . Find the output offset voltage due to V_{IO} .

Output offset = 2 mV $\times (1 + 100) = \mathbf{202$ mV. Even though the input is zero, the output has 0.2 V of error. This is why offset nulling is important in high-gain DC amplifiers.

5.2.9 Open-loop gain and closed-loop gain

Open-loop gain (A_{OL}) is the gain of the op-amp without any feedback. It is very high (2×10^5 for the 741) but also unstable and poorly controlled. A tiny differential input of only 65 μ V is enough to drive a 741 into saturation, so an op-amp without feedback is of no use as a linear amplifier. It works only as a **comparator**.

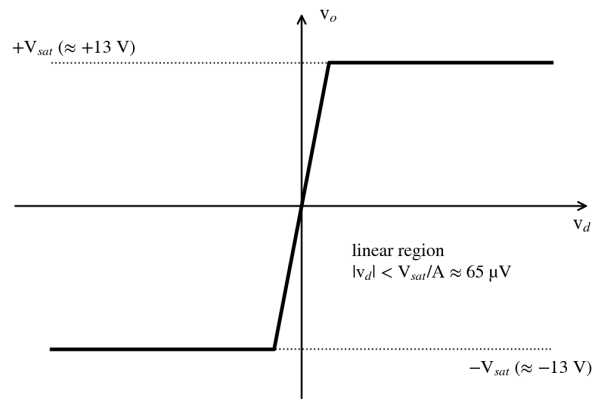


Fig. 5.8: Open-loop transfer characteristic of an op-amp

Closed-loop gain (A_{CL}) is the gain after applying negative feedback. It is much smaller than A_{OL} , but is accurately fixed by the external resistors (for example $-R_f/R_1$).

Table 5.9: Open-loop versus closed-loop operation

Property	Open loop (no feedback)	Closed loop (negative feedback)
Gain	Very high (e.g. 2×10^5), varies with temperature and supply	Lower, fixed by resistors, very stable
Operating region	Saturates for $ v_d > \sim 65 \mu V$ (switching action)	Remains in the linear region
Bandwidth	Very small (about 5 Hz for the 741)	Much larger: $f_{CL} = GBW / A_{CL}$
Distortion and noise	High	Reduced by negative feedback
Input resistance	R_i (2 M Ω)	Modified: $R_i(1 + A_{OL}B)$ for non-inverting; $\approx R_1$ for inverting
Output resistance	R_o (75 Ω)	Reduced: $R_o / (1 + A_{OL}B)$
Typical use	Comparators, zero-crossing detectors	Amplifiers, adders, integrators, filters, etc.

Gain–bandwidth trade-off: negative feedback exchanges gain for bandwidth, stability and linearity. The product of closed-loop gain and closed-loop bandwidth stays constant (see Section 5.2.12).

5.2.10 Input and output impedance (with feedback)

Negative feedback changes the input and output impedance of the op-amp. Let B be the feedback factor ($B = R_1/(R_1 + R_f)$ for the non-inverting amplifier).

Table 5.10: Input and output impedance with feedback

Quantity	Open loop (741)	Non-inverting amplifier	Inverting amplifier
Input impedance	$R_i = 2 \text{ M}\Omega$	$R_{if} = R_i (1 + A_{OL} B) \rightarrow$ extremely high	$R_{if} \approx R_1$ (fixed by the input resistor)
Output impedance	$R_o = 75 \Omega$	$R_{of} = R_o / (1 + A_{OL} B) \rightarrow$ extremely low	$R_{of} = R_o / (1 + A_{OL} B) \rightarrow$ extremely low

Example 5.6

Given: 741 ($A_{OL} = 2 \times 10^5$, $R_i = 2 \text{ M}\Omega$, $R_o = 75 \Omega$) used as a non-inverting amplifier of gain 10 ($B = 1/10$). Find R_{if} and R_{of} .
 $A_{OL} B = 2 \times 10^5 \times 0.1 = 2 \times 10^4$. $R_{if} = 2 \text{ M}\Omega \times 20001 \approx 4 \times 10^{10} \Omega$ (practically limited by leakage to a few hundred $\text{M}\Omega$). $R_{of} = 75 / 20001 \approx 3.75 \text{ m}\Omega$.

5.2.11 Slew rate

Slew rate (SR) is the **maximum rate of change of the output voltage** with time. It is specified in $\text{V}/\mu\text{s}$. For the IC 741, $\text{SR} = 0.5 \text{ V}/\mu\text{s}$. The slew rate is limited because the internal compensation capacitor C (about 30 pF) must be charged and discharged by a limited current $I_{\max}$ from the input stage:

$$\text{SR} = (dv_o / dt)_{\max} = I_{\max} / C$$

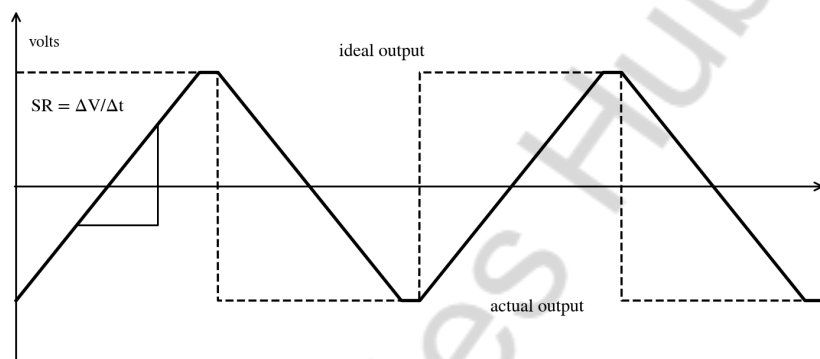


Fig. 5.9: Effect of slew-rate limiting on a square-wave response

If the input changes faster than the output can follow, the output no longer reproduces the input; a square wave becomes a trapezoid or triangle. For a sine wave $v_o = V_p \sin \omega t$ the maximum rate of change is $\omega V_p = 2\pi f V_p$. To avoid slew-rate distortion this must not exceed SR, which gives the **full-power bandwidth**:

$$f_{\max} = \text{SR} / (2\pi V_p)$$

Example 5.7

Given: $\text{SR} = 0.5 \text{ V}/\mu\text{s} = 0.5 \times 10^6 \text{ V/s}$, output peak $V_p = 10 \text{ V}$. Find the highest undistorted frequency.
 $f_{\max} = 0.5 \times 10^6 / (2\pi \times 10) \approx 7.96 \text{ kHz}$. A 741 cannot deliver an undistorted 10 V peak signal above about 8 kHz . For smaller amplitudes the usable frequency is higher.

5.2.12 Frequency response of an op-amp

The gain of an op-amp is not constant. An internal compensation capacitor produces a single **dominant pole** at a very low frequency f_1 (about 5 Hz for the 741), so the open-loop gain is:

$$A_{OL}(f) = A_0 / (1 + j f / f_1) \quad |A_{OL}(f)| = A_0 / \sqrt{1 + (f/f_1)^2}$$

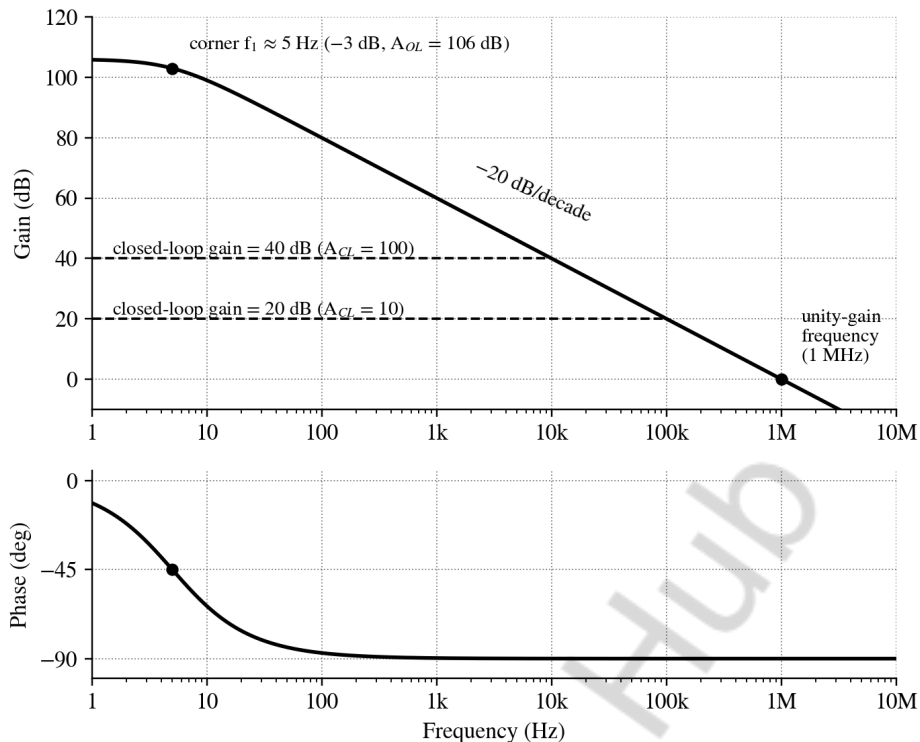


Fig. 5.10: Open-loop and closed-loop frequency response (Bode plot) of IC 741

- **Low frequencies ($f < f_1$):** the gain is constant at $A_0 = 2 \times 10^5$ (106 dB), i.e. it works down to DC.
- **At $f = f_1$:** the gain falls by 3 dB (to $0.707 A_0$) and the phase shift is -45° .
- **Above f_1 :** the gain falls at -20 dB/decade (-6 dB/octave), and the phase approaches -90° .
- **Unity-gain frequency f_t (GBW):** the frequency at which the open-loop gain is 1 (0 dB), which is 1 MHz for the 741.
- **Purpose of compensation:** without the internal capacitor, additional poles could add up to 180° phase shift while the gain is still above 1, which turns negative feedback into positive feedback and causes oscillation. Compensation keeps the amplifier **stable**.

Gain-bandwidth product: $\text{GBW} = A_0 \times f_1 = A_{\text{CL}} \times f_{\text{CL}} = \text{constant} = f_t$ (1 MHz for the 741)

Closed-loop bandwidth: $f_{\text{CL}} = \text{GBW} / A_{\text{CL}}$

Example 5.8

Given: A 741 (GBW = 1 MHz) is used as a non-inverting amplifier with $R_1 = 1 \text{ k}\Omega$, $R_f = 99 \text{ k}\Omega$. Find the bandwidth.

$A_{\text{CL}} = 1 + 99/1 = 100$. $f_{\text{CL}} = 1 \text{ MHz} / 100 = \mathbf{10 \text{ kHz}}$. Hence a gain of 100 limits the usable range to 10 kHz; a gain of 10 would give 100 kHz.

5.3 Applications of Op-Amp

Using different combinations of resistors and capacitors in the input and feedback paths, one op-amp can perform many mathematical operations. In every circuit below, the analysis uses the two golden rules ($v_+ = v_-$ and zero input current) with an ideal op-amp.

5.3.1 Adder (summing amplifier)

An adder produces an output equal to the (inverted) weighted sum of several input voltages. It is a modification of the inverting amplifier in which several input resistors are connected to the same **summing node** (virtual ground).

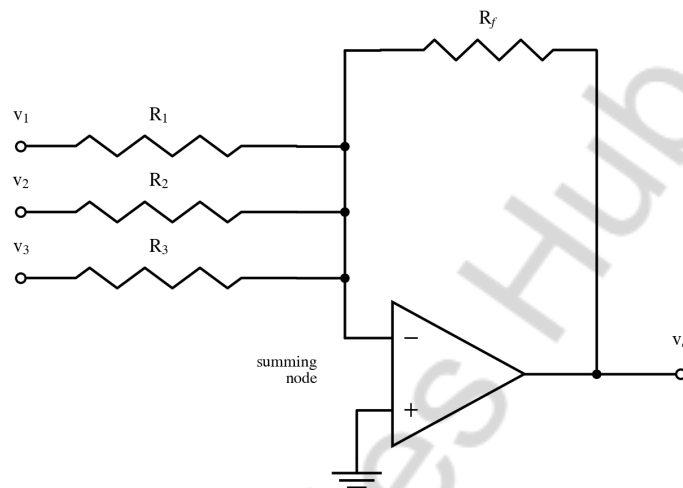


Fig. 5.11: Inverting summing amplifier (three inputs)

Derivation. The inverting node is at 0 V (virtual ground). The input currents add up and all flow through R_f :

$$i_f = i_1 + i_2 + i_3 = v_1/R_1 + v_2/R_2 + v_3/R_3$$

$$v_o = -R_f (v_1/R_1 + v_2/R_2 + v_3/R_3)$$

$$\text{If } R_1 = R_2 = R_3 = R: v_o = -(R_f/R)(v_1 + v_2 + v_3)$$

$$\text{If also } R_f = R: v_o = -(v_1 + v_2 + v_3) \quad (\text{unity-gain adder})$$

$$\text{If } R_f = R/n \text{ for } n \text{ inputs: } v_o = -(v_1 + v_2 + \dots + v_n) / n \quad (\text{averager})$$

- Each input is amplified independently by its own gain (R_f/R_n), and the inputs do **not interact** because the summing node is a virtual ground. This allows **weighted sums**, used in D/A converters and audio mixers.
- The output is inverted. To get a positive sum, an inverting amplifier ($R_f = R_1$, gain -1) can be added after the adder.
- A **non-inverting adder** is also possible by connecting the inputs, through resistors, to the non-inverting terminal.

Example 5.9

Given: $R_1 = R_2 = R_f = 10 \text{ k}\Omega$, $v_1 = 2 \text{ V}$, $v_2 = 3 \text{ V}$. Find v_o . Then find v_o when $R_1 = 5 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $R_f = 10 \text{ k}\Omega$.

$$(a) v_o = -(2 + 3) = -5 \text{ V.} \quad (b) v_o = -10k (2/5k + 3/10k) = -10k \times (0.4 \text{ mA} + 0.3 \text{ mA}) = -7 \text{ V.}$$

5.3.2 Subtractor (difference amplifier)

A subtractor gives an output proportional to the **difference** of two inputs. The circuit uses both inputs of the op-amp: v_1 goes to the inverting terminal through R_1 , and v_2 goes to the non-inverting terminal through R_2 , with R_3 to ground.

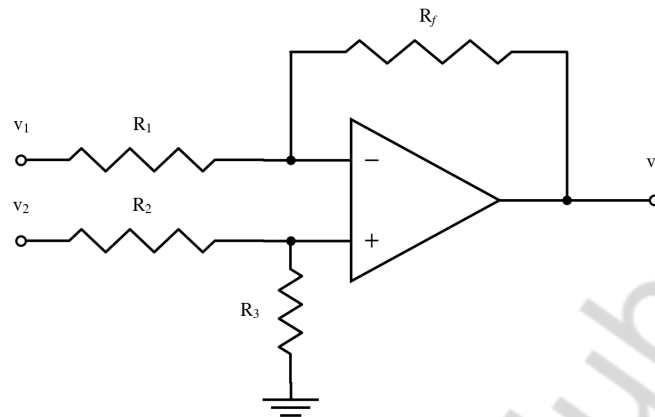


Fig. 5.12: Subtractor (difference amplifier)

Derivation (by superposition).

- **With $v_2 = 0$:** the circuit is an inverting amplifier, so $v_{o1} = -(R_f/R_1) v_1$.
- **With $v_1 = 0$:** the circuit is a non-inverting amplifier whose input is the divided voltage $v_+ = v_2 R_3/(R_2 + R_3)$.
So $v_{o2} = (1 + R_f/R_1) \cdot [R_3/(R_2 + R_3)] v_2$.
- **Total:** $v_o = v_{o1} + v_{o2}$.

$$v_o = -\left(\frac{R_f}{R_1}\right) v_1 + \left(1 + \frac{R_f}{R_1}\right) \cdot \left[\frac{R_3}{R_2 + R_3}\right] \cdot v_2$$

For matched resistors $R_1 = R_2$ and $R_f = R_3$: $v_o = \left(\frac{R_f}{R_1}\right) (v_2 - v_1)$

If $R_f = R_1$: $v_o = v_2 - v_1$ (unity-gain subtractor)

- Good matching of resistor ratios ($R_f/R_1 = R_3/R_2$) is essential for high CMRR; a 1% mismatch limits the CMRR to about 40–50 dB.
- The two inputs have **unequal input resistance** (R_1 for v_1 and $R_2 + R_3$ for v_2). Buffering the inputs with followers gives an **instrumentation amplifier**.
- Applications: bridge/sensor amplifiers, differential-signal receivers, error amplifiers in control systems.

Example 5.10

Given: $R_1 = R_2 = 1 \text{ k}\Omega$, $R_f = R_3 = 10 \text{ k}\Omega$, $v_1 = 1.2 \text{ V}$, $v_2 = 1.5 \text{ V}$. Find v_o .

$v_o = (10\text{k}/1\text{k})(1.5 - 1.2) = 10 \times 0.3 = 3 \text{ V}$.

5.3.3 Voltage follower (unity-gain buffer)

In the voltage follower the output is connected **directly** to the inverting input, and the signal is applied to the non-inverting input. This is a non-inverting amplifier with $R_f = 0$ and $R_1 = \infty$.

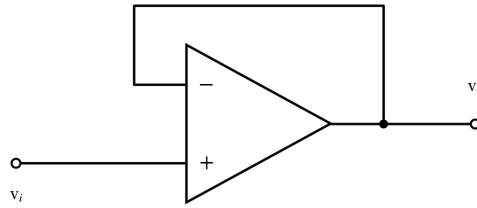


Fig. 5.13: Voltage follower

Analysis. $v_- = v_o$ (direct feedback) and $v_- = v_+ = v_i$, therefore

$v_o = v_i$	$A_{CL} = 1$ (no phase shift)	$R_{in} = \text{very high (several hundred M}\Omega\text{)}$	$R_{out} = \text{very low (milliohms)}$
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- The output “follows” the input exactly, so it is also called a **buffer** or isolation amplifier.
- Its purpose is **impedance matching**: a high-resistance source (sensor, potentiometer, filter, sample-and-hold capacitor) can drive a low-resistance load without loading error. The buffer takes almost no current from the source and supplies the current to the load.
- It has the widest bandwidth of all closed-loop configurations (equal to the unity-gain frequency, 1 MHz for the 741).
- Applications: buffers between stages, sample-and-hold circuits, active filters, voltage references and level shifters.

5.3.4 Integrator

An integrator produces an output proportional to the **time integral** of the input. It is the inverting amplifier with the feedback resistor replaced by a **capacitor** C.

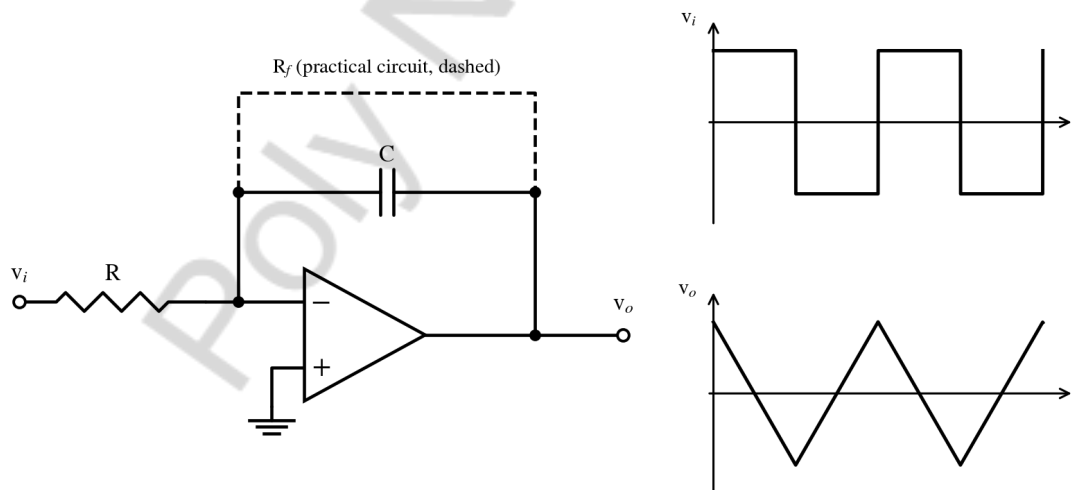


Fig. 5.14: Integrator circuit with typical input and output waveforms

Derivation. The inverting node is a virtual ground. Input current $i = v_i/R$ flows entirely into the capacitor. For a capacitor, $i = C \, d(v_C)/dt$ and $v_o = -v_C$, therefore:

$$v_o(t) = - (1 / RC) \int v_i \, dt + v_o(0)$$

Gain magnitude at frequency f : $|A_{CL}| = 1 / (2\pi f RC)$ (falls at -20 dB/decade; unity gain at $f = 1/(2\pi RC)$)

Table 5.11: Response of an integrator

Input v_i	Output v_o
Constant DC voltage V	Linear ramp: $v_o = -(V/RC) t$
Square wave	Triangular wave (inverted)
Sine wave $V_m \sin \omega t$	Cosine wave: $v_o = (V_m / \omega RC) \cos \omega t$, i.e. a 90° phase shift
Step input	Ramp, which continues until the op-amp saturates

Practical integrator. At DC, the capacitor acts as an open circuit, so the ideal integrator has an open-loop gain at DC. Even a small input offset voltage or bias current then charges the capacitor continuously and the output drifts into saturation. To avoid this, a large resistor R_f (about $10 R$) is connected in parallel with C (dashed in the figure). It limits the DC gain to R_f/R , and the circuit behaves as an integrator only for frequencies above $f_a = 1/(2\pi R_f C)$.

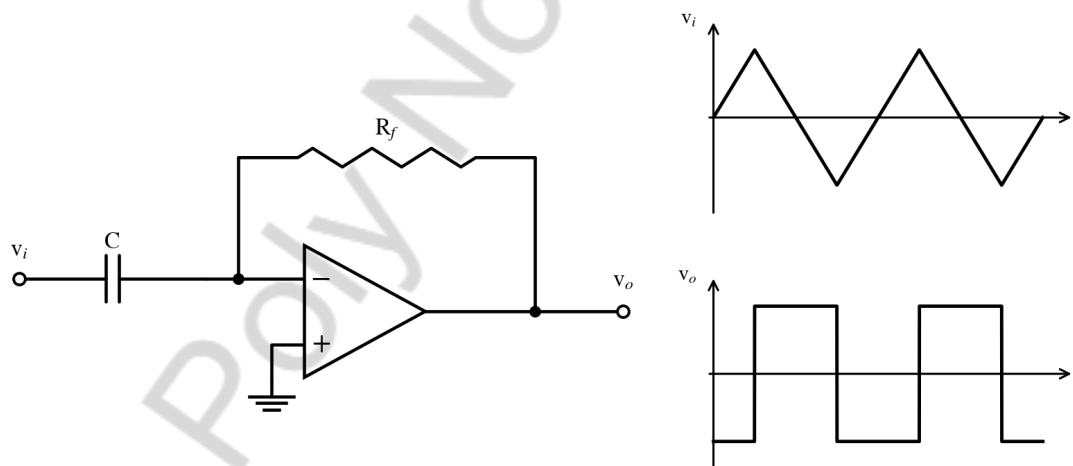
- **Applications:** triangular-wave generation from square wave, ramp (sweep) generators, analog computers (solving differential equations), A/D converters (dual-slope), active low-pass filters and PID controllers.

Example 5.11

Given: $R = 10 \text{ k}\Omega$, $C = 0.1 \text{ }\mu\text{F}$, input $v_i = +2 \text{ V DC}$ applied for 2 ms ($v_o(0) = 0$). Find v_o .
 $RC = 10 \times 10^3 \times 0.1 \times 10^{-6} = 1 \text{ ms}$. $v_o = -(1/RC) V t = -(1/1 \text{ ms})(2 \text{ V})(2 \text{ ms}) = -4 \text{ V}$.

5.3.5 Differentiator

A differentiator produces an output proportional to the **rate of change** (derivative) of the input. It is obtained by interchanging R and C of the integrator: the capacitor C is in the input path and the resistor R_f is in the feedback path.

*Fig. 5.15: Differentiator circuit with triangular input and square-wave output*

Derivation. The current through the capacitor is $i = C dv_i/dt$ (since the inverting node is at virtual ground). The same current flows through R_f so $v_o = -iR_f$:

$$v_o(t) = -R_f C \cdot dv_i / dt$$

Gain magnitude at frequency f : $|A_{CL}| = 2\pi f R_f C$ (rises at $+20 \text{ dB/decade}$)

Table 5.12: Response of a differentiator

Input v_i	Output v_o
Constant DC	Zero
Ramp (constant slope m)	Constant DC level $-R_f C m$
Triangular wave	Square wave
Square wave	Sharp positive and negative spikes at the edges
Sine wave $V_m \sin \omega t$	$-\omega R_f C V_m \cos \omega t$ (90° shifted, amplitude grows with frequency)

Practical differentiator. Because the gain increases with frequency, the ideal differentiator **amplifies high-frequency noise** and tends to be unstable (oscillation) at the point where the rising gain meets the falling open-loop gain. Two components are added: a small series resistor R_s with C limits the high-frequency gain to R_f/R_s , and a small capacitor C_f across R_f reduces the gain at very high frequency. The circuit differentiates correctly only for frequencies below $f_a = 1/(2\pi R_f C)$.

- **Applications:** wave shaping (square wave to spikes, triangular wave to square wave), rate-of-change detectors, FM demodulation, and in analog computers.

Example 5.12

Given: $R_f = 10 \text{ k}\Omega$, $C = 0.1 \text{ }\mu\text{F}$ and the input is a ramp rising at 1 V/ms . Find v_o .

$R_f C = 1 \text{ ms}$ and $dv_i/dt = 1 \text{ V/ms} = 1000 \text{ V/s}$. $v_o = -(1 \text{ ms})(1000 \text{ V/s}) = -1 \text{ V}$ (constant while the ramp lasts).

5.3.6 Comparator

A **comparator** compares an input voltage with a **reference voltage** and tells which one is larger. The op-amp is used in open loop (no feedback). Because the open-loop gain is huge, the output switches abruptly to one of the two saturation voltages:

If $v_+ > v_- \rightarrow v_o = +V_{\text{sat}}$ (positive saturation)

If $v_+ < v_- \rightarrow v_o = -V_{\text{sat}}$ (negative saturation)

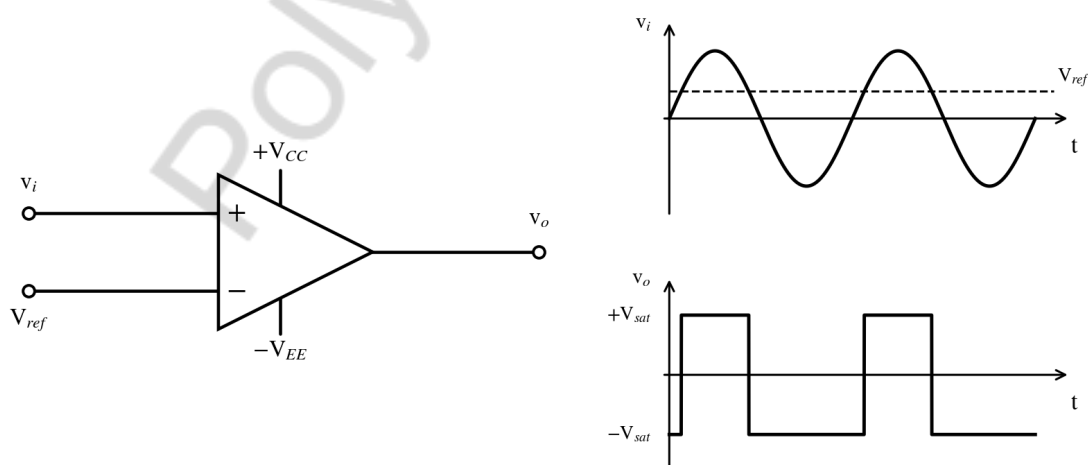


Fig. 5.16: Non-inverting comparator with reference voltage V_{ref} and its waveforms

- **Non-inverting comparator:** v_i is applied to the $+$ input and V_{ref} to the $-$ input. Output is $+V_{\text{sat}}$ when $v_i > V_{\text{ref}}$. (When $V_{\text{ref}} = 0$ it is a **zero-crossing detector**, which converts a sine wave to a square wave.)

- **Inverting comparator:** the connections are interchanged; the output is $-V_{sat}$ when $v_i > V_{ref}$.
- **Limitations:** (i) the output is limited to $\pm V_{sat}$ (about 1–2 V below the supplies); (ii) the response is slow because of slew rate and saturation recovery; (iii) if the input contains noise near the threshold, the output **chatters** (switches repeatedly), which is cured by the Schmitt trigger. Dedicated comparator ICs (LM311, LM339) are faster.
- **Applications:** zero-crossing and level detectors, square-wave generation, analog-to-digital converters, window detectors, over-voltage and under-voltage alarms, PWM generation.

5.3.7 Schmitt trigger

A **Schmitt trigger** is a comparator with **positive feedback**. The feedback creates two different threshold voltages, one for rising input and one for falling input. This difference is called **hysteresis**, and it makes the circuit immune to noise near the threshold.

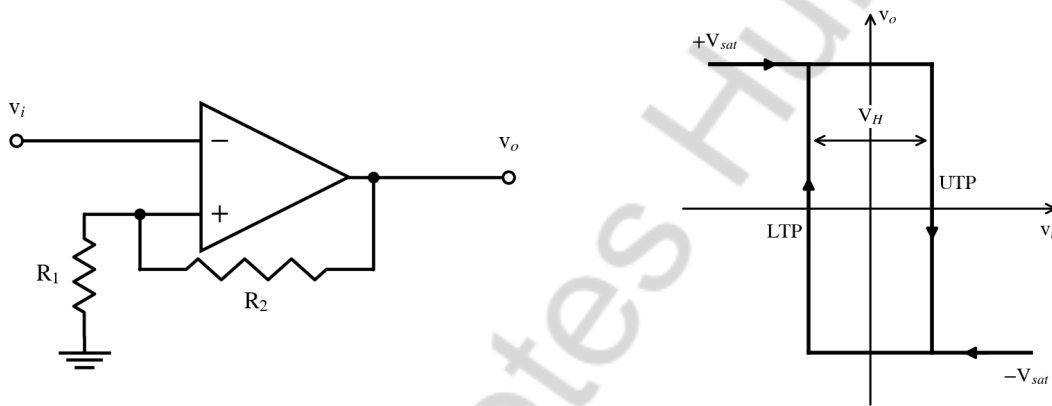


Fig. 5.17: Inverting Schmitt trigger and its transfer characteristic (hysteresis loop)

Operation (inverting Schmitt trigger). The input v_i is applied to the inverting terminal, and a fraction of the output is fed back to the non-inverting terminal through the divider R_2, R_1 . The feedback factor is:

$$\beta = R_1 / (R_1 + R_2)$$

- Suppose the output is at $+V_{sat}$. The voltage at the $+$ input is then $+\beta V_{sat}$. The output stays high until v_i rises above this value. At that moment the output flips to $-V_{sat}$. The switching level is the **upper trip point (UTP)**.
- With the output at $-V_{sat}$, the voltage at the $+$ input becomes $-\beta V_{sat}$. The output stays low until v_i falls below this value, and then it flips to $+V_{sat}$. This is the **lower trip point (LTP)**.
- Because the output change *changes the threshold* in the direction that supports the new state, the switching is very fast (regenerative action).

$$\text{UTP} = +\beta V_{sat} = +V_{sat} R_1 / (R_1 + R_2)$$

$$\text{LTP} = -\beta V_{sat} = -V_{sat} R_1 / (R_1 + R_2)$$

$$\text{Hysteresis voltage } V_H = \text{UTP} - \text{LTP} = 2\beta V_{sat} = 2V_{sat} R_1 / (R_1 + R_2)$$

Non-inverting Schmitt trigger. If the input is applied to the $+$ terminal through R_1 with R_2 as the positive-feedback resistor (the $-$ terminal grounded), the output switches in phase with the input, with trip points $\text{UTP} = +(R_1/R_2)V_{sat}$ and $\text{LTP} = -(R_1/R_2)V_{sat}$. A reference voltage can be added to shift the loop away from zero.

Table 5.13: Comparator versus Schmitt trigger

Feature	Comparator	Schmitt trigger
Feedback	None (open loop)	Positive feedback
Threshold levels	One (V_{ref})	Two (UTP and LTP)
Hysteresis	No	Yes ($V_H = 2\beta V_{sat}$)
Noise immunity	Poor; output chatters near threshold	Good; noise smaller than V_H is ignored
Applications	Level and zero-crossing detection	Squaring noisy signals, switch debouncing, relay drivers, oscillators

Example 5.13

Given: inverting Schmitt trigger with $R_1 = 1 \text{ k}\Omega$, $R_2 = 9 \text{ k}\Omega$ and $V_{sat} = \pm 12 \text{ V}$. Find UTP, LTP and V_H .
 $\beta = 1/(1 + 9) = 0.1$. UTP = $0.1 \times 12 = +1.2 \text{ V}$; LTP = -1.2 V ; $V_H = 1.2 - (-1.2) = 2.4 \text{ V}$. Any noise smaller than 2.4 V peak-to-peak on the input cannot cause false switching.

Chapter Summary: Key Formulas at a Glance

Table 5.14: Important formulas of Chapter 5

Topic	Formula / result
Diff-amp bias	$I_E = (V_{EE} - V_{BE}) / (2R_E)$ per transistor; $r_e = 26 \text{ mV} / I_E$
Diff-amp gain	A_d (balanced) = R_C / r_e ; A_d (single-ended) = $R_C / 2r_e$; $A_c \approx -R_C / 2R_E$; $\text{CMRR} \approx R_E / r_e$
Ideal op-amp rules	$v_+ = v_-$; $i_+ = i_- = 0$
Inverting amplifier	$A_{CL} = -R_f / R_1$; $R_{in} = R_1$
Non-inverting amplifier	$A_{CL} = 1 + R_f / R_1$; R_{in} very high
CMRR	$\text{CMRR} = A_d / A_c $; in dB = $20 \log_{10} A_d / A_c $
Bias and offset currents	$I_B = (I_{B1} + I_{B2}) / 2$; $I_{IO} = I_{B1} - I_{B2} $; $R_{comp} = R_1 \parallel R_f$
Output offset	$V_{IO}(1 + R_f / R_1) + I_{IO} R_f$
Slew rate	$SR = dv_o / dt _{\max} = I / C$; $f_{\max} = SR / (2\pi V_p)$
Bandwidth	$GBW = A_{CL} \times f_{CL} = 1 \text{ MHz (741)}$; $f_{CL} = GBW / A_{CL}$
Impedance with feedback	$R_{if} = R_i(1 + A_{OL} B)$ (non-inv); $R_{of} = R_o / (1 + A_{OL} B)$
Adder	$v_o = -R_f(v_1 / R_1 + v_2 / R_2 + v_3 / R_3)$
Subtractor	$v_o = (R_f / R_1)(v_2 - v_1)$ for $R_1 = R_2$, $R_f = R_3$
Voltage follower	$v_o = v_i$
Integrator	$v_o = -(1/RC) \int v_i dt$
Differentiator	$v_o = -R_f C dv_i / dt$
Comparator	$v_o = +V_{sat}$ if $v_+ > v_-$, else $-V_{sat}$
Schmitt trigger	$UTP = +\beta V_{sat}$; $LTP = -\beta V_{sat}$; $V_H = 2\beta V_{sat}$; $\beta = R_1 / (R_1 + R_2)$

Multiple Choice Questions (15 MCQs)

Choose the correct option. The answer key with short explanations is given after the questions.

Q1. A differential amplifier amplifies mainly the

- (a) sum of the two inputs
- (b) difference of the two inputs
- (c) product of the two inputs
- (d) average of the two inputs

Q2. The CMRR of an ideal op-amp is

- (a) zero
- (b) unity
- (c) 100 dB
- (d) infinity

Q3. An inverting amplifier has $R_1 = 2 \text{ k}\Omega$ and $R_f = 20 \text{ k}\Omega$. Its voltage gain is

- (a) +10
- (b) -0.1
- (c) -10
- (d) +11

Q4. A non-inverting amplifier has $R_1 = 1 \text{ k}\Omega$ and $R_f = 9 \text{ k}\Omega$. Its voltage gain is

- (a) 10
- (b) 9
- (c) -10
- (d) 0.1

Q5. The term “virtual ground” in an inverting amplifier means that the inverting terminal is

- (a) directly connected to ground
- (b) at ground potential but draws no current to ground
- (c) at the negative supply voltage
- (d) at the positive supply voltage

Q6. The unit of slew rate is

- (a) V/ μ s
- (b) A/ μ s
- (c) Hz/V
- (d) dB/decade

Q7. Input offset voltage is the voltage that must be applied between the input terminals to

- (a) increase the gain
- (b) increase the bandwidth
- (c) make the output voltage zero
- (d) make the output voltage maximum

Q8. For an adder with $R_1 = R_2 = R_3 = R_f$, the output voltage is

- (a) $v_1 + v_2 + v_3$
- (b) $(v_1 + v_2 + v_3)/3$
- (c) $-(v_1 + v_2 + v_3)/R$
- (d) $-(v_1 + v_2 + v_3)$

- Q9.** A 741 (GBW = 1 MHz) is used with a closed-loop gain of 100. The approximate bandwidth is
- (a) 100 kHz
 - (b) 10 kHz
 - (c) 1 MHz
 - (d) 100 Hz
- Q10.** An op-amp circuit with voltage gain 1, very high input resistance and very low output resistance is called a
- (a) integrator
 - (b) differentiator
 - (c) voltage follower
 - (d) comparator
- Q11.** When a constant DC voltage is applied to an ideal integrator, the output is
- (a) a linear ramp
 - (b) a constant DC voltage
 - (c) a sine wave
 - (d) zero
- Q12.** If a triangular wave is applied to an ideal differentiator, the output is a
- (a) triangular wave
 - (b) sine wave
 - (c) DC level
 - (d) square wave
- Q13.** An op-amp used as a comparator works
- (a) with negative feedback
 - (b) with positive feedback
 - (c) in open loop (no feedback)
 - (d) only for sine inputs
- Q14.** Input offset current of an op-amp is the
- (a) difference between the two input bias currents
 - (b) sum of the two input bias currents
 - (c) average of the two input bias currents
 - (d) product of the two input bias currents
- Q15.** An inverting Schmitt trigger has $R_1 = 1 \text{ k}\Omega$, $R_2 = 9 \text{ k}\Omega$ and $V_{\text{sat}} = \pm 10 \text{ V}$. The upper trip point is
- (a) +0.1 V
 - (b) +1 V
 - (c) +9 V
 - (d) +10 V

Answer Key for MCQs

Q.	Ans.	Explanation
1	(b)	It amplifies $v_d = v_1 - v_2$ and rejects the common part.
2	(d)	$A_c = 0$ for an ideal op-amp, so $A_d/A_c = \infty$.
3	(c)	$A_{CL} = -R_f/R_1 = -20/2 = -10$.
4	(a)	$A_{CL} = 1 + R_f/R_1 = 1 + 9 = 10$.
5	(b)	Since $v_+ = 0$ and $v_- = v_+$, the node is at 0 V, but it cannot sink current.
6	(a)	Slew rate is the maximum rate of change of output voltage, e.g. 0.5 V/ μ s for the 741.
7	(c)	It nulls the output error caused by mismatch in the input stage.
8	(d)	$v_o = -(R_f/R)(v_1 + v_2 + v_3)$ with $R_f = R$.
9	(b)	$f_{CL} = \text{GBW} / A_{CL} = 1 \text{ MHz} / 100 = 10 \text{ kHz}$.
10	(c)	In a voltage follower $v_o = v_i$; it is used as a buffer.
11	(a)	$v_o = -(V/RC)t$, a linearly changing voltage.
12	(d)	The derivative of a triangular wave is constant (positive or negative) in each half cycle, giving a square wave.
13	(c)	The huge open-loop gain drives the output to $\pm V_{\text{sat}}$.
14	(a)	$I_{IO} = I_{B1} - I_{B2} $.
15	(b)	$\beta = 1/(1 + 9) = 0.1$, so $\text{UTP} = 0.1 \times 10 = +1 \text{ V}$.

Quick key: 1-b, 2-d, 3-c, 4-a, 5-b, 6-a, 7-c, 8-d, 9-b, 10-c, 11-a, 12-d, 13-c, 14-a, 15-b

Broad Questions (10 Long-Answer Questions)

- Q1.** Draw the circuit of a BJT differential amplifier and explain its operation for (i) differential input and (ii) common-mode input. Derive the expressions for A_d (dual-input, balanced-output) and the CMRR.
- Q2.** Describe the four configurations of a differential amplifier. Compare them with respect to the differential gain, input resistance and output resistance. Why is a constant current source used in place of R_E ?
- Q3.** Draw the block diagram of an operational amplifier and explain the function of each block. List the characteristics of an ideal op-amp and compare them with those of the IC 741.
- Q4.** What is virtual ground? Derive the expression for the closed-loop gain of an inverting amplifier using the virtual ground concept. Design an inverting amplifier of gain -25 with an input resistance of $10\text{ k}\Omega$, and find the output for an input of 0.2 V .
- Q5.** Derive the voltage gain of a non-inverting amplifier. Compare the inverting and non-inverting amplifiers. Design a non-inverting amplifier of gain 11 using $R_1 = 1\text{ k}\Omega$.
- Q6.** Define and explain: (i) CMRR, (ii) input bias current, (iii) input offset current, (iv) input offset voltage and (v) slew rate. State their typical values for the IC 741 and describe how the effect of bias current and offset voltage is minimised.
- Q7.** Explain the frequency response of an op-amp with a neat sketch. Distinguish between open-loop and closed-loop gain, define gain–bandwidth product, and calculate the closed-loop bandwidth of a 741 ($\text{GBW} = 1\text{ MHz}$) for a gain of 50 . Also explain how the input and output impedance change with feedback.
- Q8.** With circuit diagrams, derive the output expressions of (i) an inverting adder and (ii) a subtractor (difference amplifier). Find the output of an adder with $R_1 = 10\text{ k}\Omega$, $R_2 = 20\text{ k}\Omega$, $R_f = 20\text{ k}\Omega$, $v_1 = 1\text{ V}$ and $v_2 = 2\text{ V}$.
- Q9.** Explain the working of an ideal integrator and a differentiator using circuit diagrams and derive their output equations. Sketch the output waveforms for square and triangular inputs and state the practical limitations and the modifications made to the circuits.
- Q10.** Draw the circuit of an inverting Schmitt trigger and explain its operation with the transfer characteristic. Derive the expressions for UTP, LTP and hysteresis voltage. Compare the Schmitt trigger with an ordinary comparator and give two applications.

End of Chapter 5 – Operational Amplifier