

ELECTRONICS DEVICES & CIRCUITS

CHAPTER 6

TIMER CIRCUITS

Study Notes for Engineering Students

Theory, Diagrams, Worked Examples, 15 MCQs and 10 Broad Questions

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- 6.1 Principle of Operation of Electronic Timer
- 6.2 Functional Description of Internal Blocks of Timer IC 555
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Chapter 6: Timer Circuits

Overview. Almost every electronic system needs to measure, generate or control time. A washing machine must run its wash cycle for a fixed duration, a traffic light must change colour at regular intervals, a microcontroller needs a clock, and a burglar alarm must sound for a limited time. Circuits that perform these jobs are called **timer circuits**. This chapter explains how a timer works in principle, studies the most popular timer integrated circuit, the **IC 555**, shows how to use it as a one-shot (monostable) and as a free-running (astable) pulse generator, and finally introduces the principle of the **digital timer**, which measures time by counting clock pulses.

Learning objectives. After studying this chapter the student will be able to:

- explain the working principle of an electronic timer using RC charging;
- draw and describe the internal block diagram of the IC 555 and state the function of each block;
- design and analyse the 555 in monostable and astable modes using the standard formulas;
- explain the block diagram and operation of a digital timer and compare it with an analog timer;
- solve numerical problems on pulse width, frequency, duty cycle and clock counts.

6.1 Principle of Operation of Electronic Timer

6.1.1 Introduction

A **timer** is a circuit or device that either (i) produces a change at its output after a pre-determined interval of time has elapsed since it was started, or (ii) produces a continuous train of pulses with a definite repetition rate. An **electronic timer** does this without moving mechanical parts; the time interval is set by the charging or discharging of a capacitor through a resistor (analog timer) or by counting pulses of a stable clock (digital timer).

Some common terms used while studying timers are given below.

Term	Meaning	Symbol / Unit
Delay time	Time between the start (trigger) and the change of the output.	t_d , seconds
Pulse width	Duration for which the output stays in its active (HIGH) state.	T or t_H , seconds
Period	Time of one complete cycle of a repetitive waveform ($t_H + t_L$).	T, seconds
Frequency	Number of cycles per second; $f = 1 / T$.	f, hertz (Hz)
Duty cycle	Ratio of HIGH time to the total period, usually in percent: $D = t_H / T \times 100 \%$.	D, %
Time constant	Product of resistance and capacitance of the timing network.	$\tau = RC$, seconds

6.1.2 Need and Applications of Timers

Timers are used wherever an action must be delayed, lengthened, repeated or sequenced. Typical applications are:

- time-delay relays and motor start/stop sequencing in industrial control;
- pulse generation, clock generation and frequency division in digital systems;
- LED flashers, buzzers, sirens and tone generators;
- automatic staircase and corridor lights, washing machines, microwave ovens and toasters;
- pulse-width modulation (PWM) for speed control and dimming;
- debouncing of mechanical switches and missing-pulse detection.

6.1.3 Classification of Timers

Timers may be classified according to the method used to create the time interval. The table below compares the main types.

Type	Principle of timing	Typical use	Remarks
Electromechanical (clockwork / motor-driven)	Gear train, spring or small synchronous motor rotates a cam.	Old washing machines, geysers	Moving parts, wear, limited accuracy, bulky
Thermal (bimetal)	Heating of a bimetallic strip bends it and opens a contact.	Fan regulators, flashers	Slow, temperature dependent
Analog electronic (RC timer)	Capacitor charges through a resistor until a threshold is reached.	Short delays, one-shots, oscillators	Simple and cheap; accuracy depends on R, C tolerance

Type	Principle of timing	Typical use	Remarks
IC timer (e.g. 555)	RC network with comparators, flip-flop and output stage in one IC.	Monostable and astable circuits	Stable, flexible, very popular
Digital timer	Counting of pulses from a crystal or mains clock.	Clocks, process timers, ovens	Very accurate, long ranges, digital display

6.1.4 Block Diagram of a Basic Electronic Timer

Every electronic timer, whatever its internal circuit, can be represented by four functional blocks shown in Fig. 6.1.

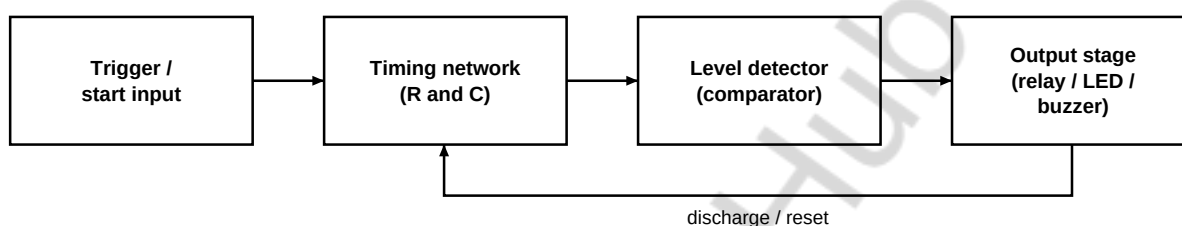


Fig. 6.1: Block diagram of a basic electronic timer

- **Trigger / start input:** a pulse, a switch closure or a voltage level that starts the timing action.
- **Timing network:** a resistor–capacitor pair whose time constant decides the length of the interval.
- **Level detector:** a comparator that senses when the capacitor voltage reaches a fixed reference level and so marks the end of the interval.
- **Output stage:** a switch or buffer that drives the load (relay, LED, buzzer or the next logic stage); it also resets the timing network by discharging the capacitor.

6.1.5 RC Timing Principle

The basic idea of an analog electronic timer is that a capacitor cannot change its voltage instantly. When a step voltage V_s is applied to a resistor R in series with an uncharged capacitor C , the capacitor voltage rises **exponentially** according to

$$v_c(t) = V_s (1 - e^{-t/RC})$$

The quantity $\tau = RC$ is called the **time constant**. After one time constant the capacitor has charged to 63.2 % of the supply; after five time constants it is practically fully charged (99.3 %). Fig. 6.2 shows the charging curve and Table 6.1 lists the percentage charge.

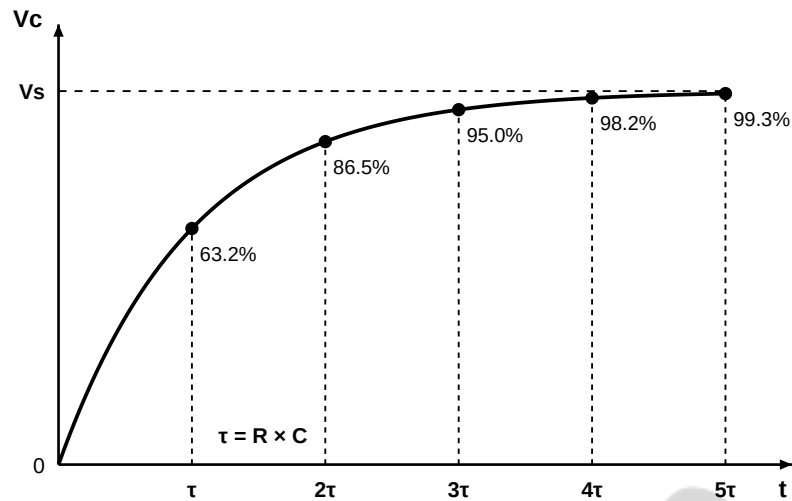


Fig. 6.2: Charging of a capacitor through a resistor (RC charging curve)

Time (t)	0.5 τ	1 τ	2 τ	3 τ	4 τ	5 τ
Capacitor voltage, % of V_s	39.3	63.2	86.5	95.0	98.2	99.3

Table 6.1: Capacitor charging with time

If a comparator is arranged to change state when the capacitor voltage reaches a threshold V_{th} , the **delay time** is found by solving the charging equation for t:

$$t_d = RC \cdot \ln [V_s / (V_s - V_{th})]$$

The two thresholds most often used in timers give the following results.

Threshold V_{th}	Value of ln term	Delay time t_d
$\frac{1}{2} V_s$	$\ln 2 = 0.693$	0.693 RC
$\frac{2}{3} V_s$	$\ln 3 = 1.0986$	1.1 RC (approximately)

Why ratio-based thresholds? In the IC 555 the threshold levels are fixed fractions ($\frac{1}{3}$ and $\frac{2}{3}$) of the supply voltage V_{CC} , and the charging source is also V_{CC} . Because both scale together, the time interval depends only on R and C and is almost independent of the supply voltage. This is the main reason for the excellent stability of 555-based timers.

6.1.6 Modes of Timer Operation

Depending on how the output behaves, timer circuits work in three modes.

Mode	Stable states	Triggering	Output	Example
Monostable (one-shot)	One	Needs one trigger pulse for every operation	A single pulse of fixed width, then returns to the stable state	Time-delay relay, touch switch
Astable (free-running)	None	No trigger needed	Continuous rectangular wave; width and frequency set by R and C	Clock generator, LED flasher, siren
Bistable	Two	Separate set and reset inputs	Stays in either state until the opposite trigger arrives	Latch, flip-flop, memory element

6.1.7 Advantages and Limitations of Electronic Timers

Advantages

- no moving parts, hence long life, silent operation and high reliability;
- time interval can be changed easily by changing R or C;
- small size, low cost and very low power consumption;
- can be triggered electronically and interfaced directly with logic circuits.

Limitations

- accuracy of an RC timer is limited by the tolerance, temperature drift and leakage of R and C (electrolytic capacitors are especially poor for long delays);
- very long delays need very large R and C values, which become impractical (digital timers are preferred then).

Worked Example 6.1

A capacitor of $10\ \mu\text{F}$ is charged through $100\ \text{k}\Omega$ from a supply, and a comparator trips at $\frac{2}{3}$ of the supply. Find the delay.

Solution: $\tau = RC = 100 \times 10^3 \times 10 \times 10^{-6} = 1\ \text{s}$.

$t_d = 1.1 RC = 1.1 \times 1 = \mathbf{1.1\ \text{s}}$ (exactly 1.0986 s).

Key Points of Section 6.1

- An electronic timer uses the exponential charging of an RC network and a comparator to fix a time interval.
- Time constant $\tau = RC$; capacitor reaches 63.2 % of the supply in one τ .
- Delay to $\frac{2}{3} V_s$ is $1.1 RC$ and to $\frac{1}{2} V_s$ is $0.693 RC$.
- Modes: monostable (one stable state), astable (no stable state), bistable (two stable states).

6.2 Functional Description of Internal Blocks of Timer IC 555

6.2.1 Introduction to the IC 555

The 555 timer was designed by Hans Camenzind and introduced by Signetics in 1972. The popular bipolar version is known as **NE555**. It is an 8-pin integrated circuit that contains about 25 transistors, two diodes and 15 resistors. It can operate as a precise time-delay generator or as an oscillator, with timing intervals ranging from microseconds to many minutes, using only a few external resistors and capacitors. The name “555” comes from the three equal 5 kΩ resistors used in its internal voltage divider.

6.2.2 Main Features

- supply voltage range of about 4.5 V to 16 V (single supply), so it can work directly from a 5 V logic supply;
- output can source or sink a current of up to about 200 mA, enough to drive a relay, LED or small speaker;
- output levels are compatible with TTL logic when operated from 5 V;
- adjustable duty cycle and timing from microseconds up to hours;
- good temperature stability (typically of the order of 50 ppm per °C) and nearly supply-independent timing;
- operates as monostable or astable multivibrator with very few external components;
- available in 8-pin DIP or SMD packages; typical maximum frequency of a few hundred kHz.

6.2.3 Pin Diagram and Pin Functions

Fig. 6.3 shows the top view of the 8-pin package. Pin 1 is identified by the notch (or dot) on the package.

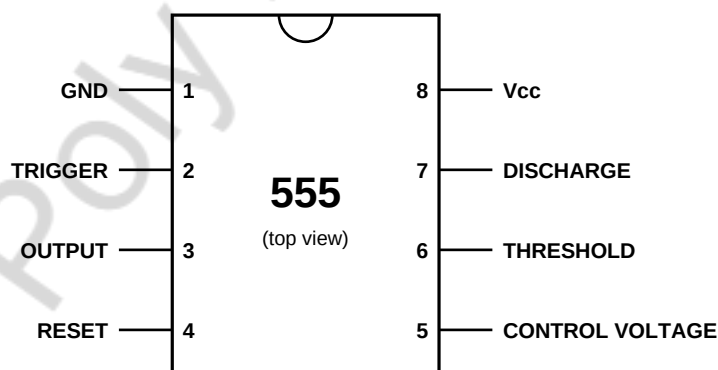


Fig. 6.3: Pin diagram of IC 555 (top view)

Pin	Name	Function
1	Ground (GND)	Common return of the supply; 0 V reference.
2	Trigger	Input to the lower comparator. When this pin voltage falls below $\frac{1}{3} V_{CC}$, the flip-flop is set and the output goes HIGH. Starts the timing in monostable mode.

Pin	Name	Function
3	Output	Totem-pole output stage. HIGH is about 1.7 V below V_{CC} , LOW is close to 0 V; sinks or sources up to about 200 mA.
4	Reset	Active-low input. When pulled below about 0.4 V it overrides all other inputs and forces the output LOW. Connected to V_{CC} if not used.
5	Control voltage	Gives access to the $\frac{2}{3} V_{CC}$ reference point. Used to change the thresholds externally; normally bypassed to ground with a 0.01 μ F capacitor to avoid noise.
6	Threshold	Input to the upper comparator. When this pin voltage rises above $\frac{2}{3} V_{CC}$, the flip-flop is reset and the output goes LOW.
7	Discharge	Open-collector terminal of the internal NPN transistor. Provides a discharge path for the external timing capacitor.
8	V_{CC}	Positive supply voltage (4.5 V to 16 V).

6.2.4 Internal Block Diagram

The IC consists of a voltage divider, two comparators, an SR flip-flop, a discharge transistor and an output stage. Their interconnection is shown in Fig. 6.4.

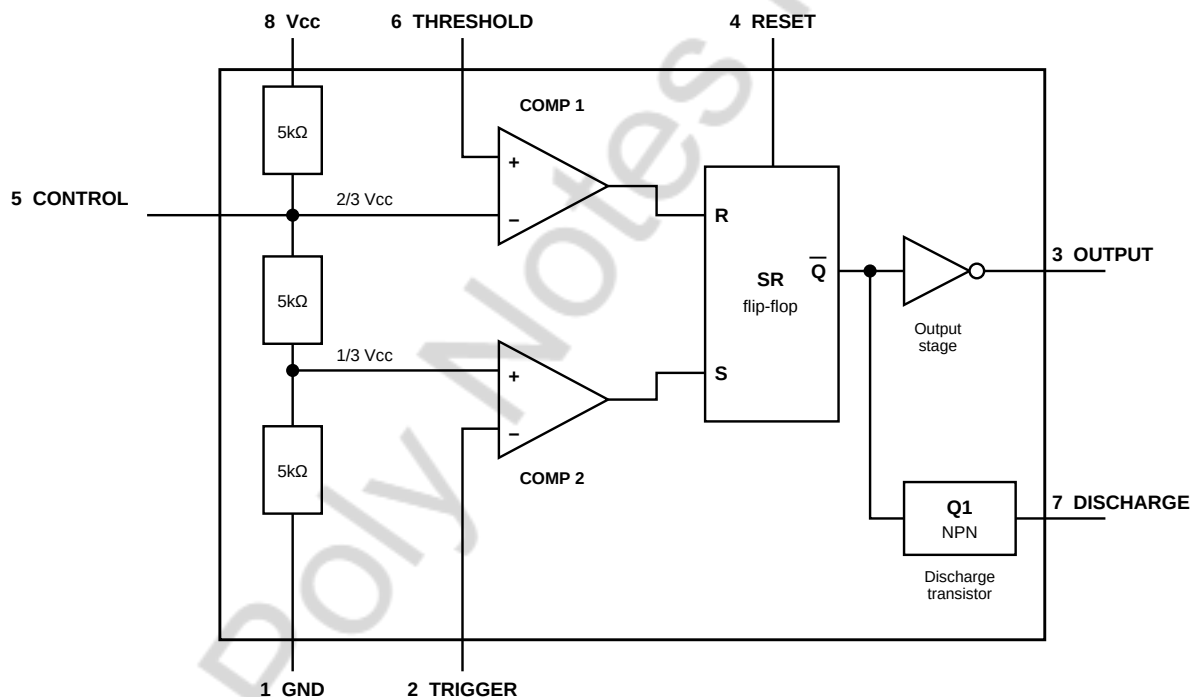


Fig. 6.4: Internal block diagram of IC 555

6.2.5 Function of Each Internal Block

(a) Resistive voltage divider

Three equal resistors of 5 k Ω each are connected in series between V_{CC} and ground. They create two reference voltages: $\frac{2}{3} V_{CC}$ at the upper junction and $\frac{1}{3} V_{CC}$ at the lower junction. The total divider resistance is 15 k Ω , so the divider draws a small standing current of $V_{CC} / 15 \text{ k}\Omega$ (about 0.33 mA at 5 V). Since the references are fixed fractions of the supply, the timing accuracy does not depend much on the supply voltage.

(b) Comparator 1 – threshold comparator

Its non-inverting (+) input is the **threshold pin 6** and its inverting (–) input is held at $\frac{2}{3} V_{CC}$. The output becomes HIGH when the voltage at pin 6 exceeds $\frac{2}{3} V_{CC}$. This HIGH output is applied to the **reset (R)** input of the flip-flop.

(c) Comparator 2 – trigger comparator

Its inverting (–) input is the **trigger pin 2** and its non-inverting (+) input is held at $\frac{1}{3} V_{CC}$. The output becomes HIGH when the voltage at pin 2 falls below $\frac{1}{3} V_{CC}$. This HIGH output is applied to the **set (S)** input of the flip-flop.

(d) SR flip-flop

The flip-flop is the memory element of the timer. A HIGH on S sets it ($Q = 1$) and a HIGH on R resets it ($Q = 0$). When both comparator outputs are LOW the flip-flop **holds** its previous state. The output of the flip-flop decides the state of the output pin 3 and of the discharge transistor. The external reset pin 4 acts directly on the flip-flop and has priority over both comparators.

(e) Discharge transistor (Q1)

This is an NPN transistor whose collector is brought out at pin 7 and whose emitter is grounded. It is driven by the complement of Q (written Q'). When the flip-flop is reset (output LOW), Q1 conducts and quickly discharges the external timing capacitor. When the flip-flop is set (output HIGH), Q1 is OFF and the capacitor is free to charge.

(f) Output stage

A buffer (totem-pole) amplifier follows the flip-flop. It increases the current capability to about 200 mA and inverts the flip-flop signal Q' , so that a **set** flip-flop gives a **HIGH** output at pin 3.

(g) Control voltage pin 5

Pin 5 is connected to the $\frac{2}{3} V_{CC}$ point of the divider. If an external voltage V_C is applied to this pin, the upper threshold becomes V_C and the lower threshold becomes $V_C/2$. This is used for pulse-width modulation and frequency modulation (voltage-controlled oscillator). When it is not used, a 0.01 μF capacitor is connected from pin 5 to ground to bypass noise.

6.2.6 Operation of the Internal Blocks – Summary Table

Condition at inputs	Comp. 1 (R)	Comp. 2 (S)	Flip-flop	Output (pin 3)	Discharge transistor
Trigger $< \frac{1}{3} V_{CC}$ (threshold below $\frac{2}{3} V_{CC}$)	LOW	HIGH	Set	HIGH	OFF
Threshold $> \frac{2}{3} V_{CC}$ (trigger above $\frac{1}{3} V_{CC}$)	HIGH	LOW	Reset	LOW	ON
Trigger $> \frac{1}{3} V_{CC}$ and threshold $< \frac{2}{3} V_{CC}$	LOW	LOW	No change (memory)	Previous state	Previous state
Reset pin 4 pulled LOW	X	X	Forced reset	LOW	ON

6.2.7 Family of 555 Timers

Device	Description
NE555 / LM555	Standard single bipolar timer in 8-pin package.
NE556	Two independent 555 timers in one 14-pin package (dual timer).

Device	Description
NE558	Four timers in one 16-pin package (quad timer).
LMC555 / TLC555 / 7555	CMOS versions: very low supply current, work at low supply voltages (down to about 2 V), higher input impedance, but lower output current.

Key Points of Section 6.2

- Internal blocks: $3 \times 5 \text{ k}\Omega$ divider, two comparators, SR flip-flop, discharge transistor, output stage.
- Reference levels: threshold comparator at $\frac{2}{3} V_{CC}$, trigger comparator at $\frac{1}{3} V_{CC}$.
- Trigger below $\frac{1}{3} V_{CC}$ sets the output HIGH; threshold above $\frac{2}{3} V_{CC}$ resets it LOW.
- Discharge transistor is ON whenever the output is LOW; reset pin 4 is active-low.

6.3 Use of 555 Timers in Monostable and Astable Mode

6.3.1 Monostable Multivibrator (One-Shot)

A monostable multivibrator has **one stable state**. When a trigger pulse is applied, it goes to a quasi-stable state for a time T fixed by R and C and then returns by itself to the stable state. Fig. 6.5 shows the 555 connected as a monostable multivibrator.

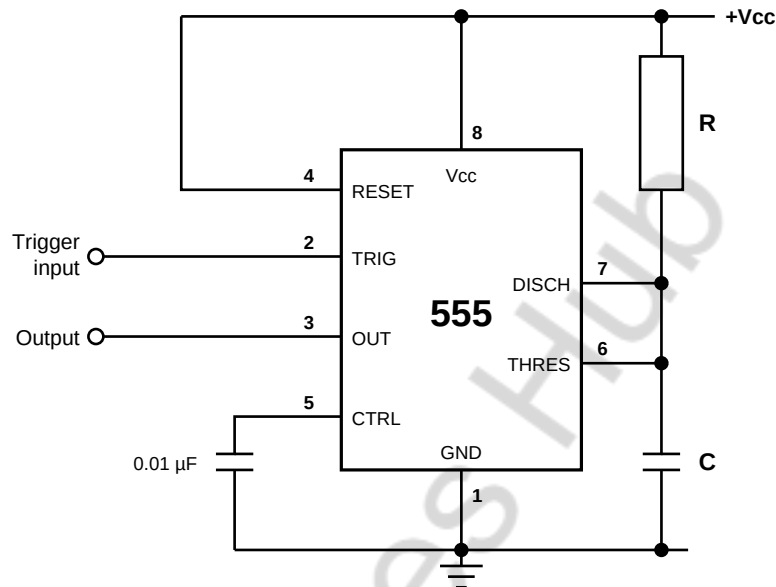


Fig. 6.5: IC 555 as a monostable multivibrator

Circuit connections

- a resistor R is connected between V_{CC} and the junction of pins 6 and 7;
- a timing capacitor C is connected from this junction (pins 6 and 7) to ground;
- the trigger input is applied to pin 2 (it is normally kept HIGH, above $\frac{1}{3} V_{CC}$);
- pin 4 is tied to V_{CC} , pin 5 is bypassed to ground through $0.01 \mu\text{F}$, and the output is taken from pin 3.

Working

1. **Stable state.** With no trigger, the flip-flop is in the reset state. The output is LOW and the discharge transistor Q_1 is ON, so pin 7 holds the capacitor voltage at about 0 V.
2. **Triggering.** A negative-going pulse at pin 2 takes the trigger voltage below $\frac{1}{3} V_{CC}$. Comparator 2 sets the flip-flop; the output goes HIGH and Q_1 turns OFF.
3. **Timing.** The capacitor now charges from V_{CC} through R . The output stays HIGH during this time (quasi-stable state).
4. **End of pulse.** When the capacitor voltage reaches $\frac{2}{3} V_{CC}$, comparator 1 resets the flip-flop. The output returns LOW, Q_1 turns ON and the capacitor discharges rapidly. The circuit is again ready for the next trigger.

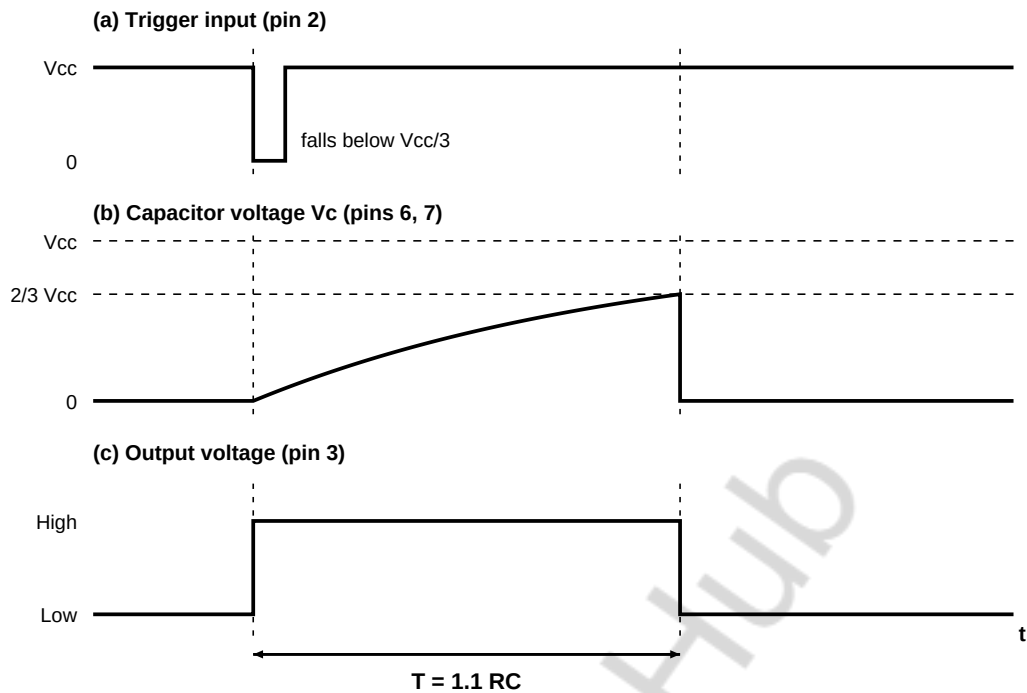


Fig. 6.6: Waveforms of the monostable multivibrator

Pulse width. The capacitor charges from 0 to $\frac{2}{3} V_{CC}$ through R . Putting $V_{th} = \frac{2}{3} V_{CC}$ in the charging equation gives

$$T = RC \ln 3 = 1.0986 RC \approx 1.1 RC$$

The width depends only on R and C and not on the supply voltage or on the trigger pulse width, provided the trigger pulse is **shorter** than T . If the trigger stays LOW for longer than T , the output will remain HIGH until the trigger returns above $\frac{1}{3} V_{CC}$. Typical timing components: R from about $1 \text{ k}\Omega$ to $10 \text{ M}\Omega$ and C from about 100 pF upwards.

R	C	Pulse width $T = 1.1 RC$
$10 \text{ k}\Omega$	$0.1 \mu\text{F}$	1.1 ms
$100 \text{ k}\Omega$	$1 \mu\text{F}$	0.11 s
$10 \text{ k}\Omega$	$10 \mu\text{F}$	0.11 s
$1 \text{ M}\Omega$	$10 \mu\text{F}$	11 s

Worked Example 6.2

Design a monostable timer that keeps a lamp ON for 2 s. Take $C = 100 \mu\text{F}$.

Solution: $T = 1.1 RC$, so $R = T / (1.1 C) = 2 / (1.1 \times 100 \times 10^{-6}) = 2 / (1.1 \times 10^{-4}) \approx 18.2 \text{ k}\Omega$.

Use the nearest standard value, **$R = 18 \text{ k}\Omega$** (a trimmer pot in series helps to fine tune the time).

Applications of monostable mode:

- time-delay circuits, relay hold-on and automatic light switches;
- touch switch and push-button timers;
- missing-pulse detector and frequency divider;

- pulse stretching, pulse-width modulation and switch debouncing.

6.3.2 Astable Multivibrator (Free-Running Oscillator)

An astable multivibrator has **no stable state**. The output switches continuously between HIGH and LOW, producing a rectangular wave without any external trigger. Fig. 6.7 shows the 555 connected as an astable multivibrator.

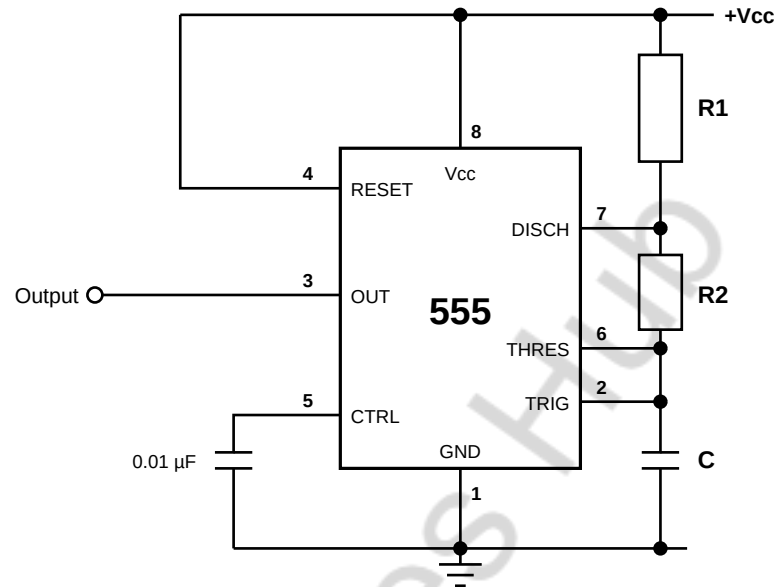


Fig. 6.7: IC 555 as an astable multivibrator

Circuit connections

- two resistors R_1 and R_2 are connected in series between V_{CC} and pin 6; the junction of R_1 and R_2 is connected to the discharge pin 7;
- the timing capacitor C is connected from pin 6 to ground; pins 2 and 6 are joined together, so the capacitor voltage is applied to both comparators;
- pin 4 is tied to V_{CC} , pin 5 is bypassed with $0.01 \mu\text{F}$, and the output is taken from pin 3.

Working

1. **Charging (output HIGH).** When the capacitor voltage is below $\frac{1}{3} V_{CC}$ the flip-flop is set, the output is HIGH and Q1 is OFF. The capacitor charges from V_{CC} through $R_1 + R_2$.
2. **Upper threshold.** When the capacitor voltage reaches $\frac{2}{3} V_{CC}$, comparator 1 resets the flip-flop. The output goes LOW and Q1 turns ON.
3. **Discharging (output LOW).** The capacitor now discharges through R_2 and the transistor Q1 into ground. Resistor R_1 is not in the discharge path.
4. **Lower threshold.** When the capacitor voltage falls to $\frac{1}{3} V_{CC}$, comparator 2 sets the flip-flop again, the output becomes HIGH and the cycle repeats.

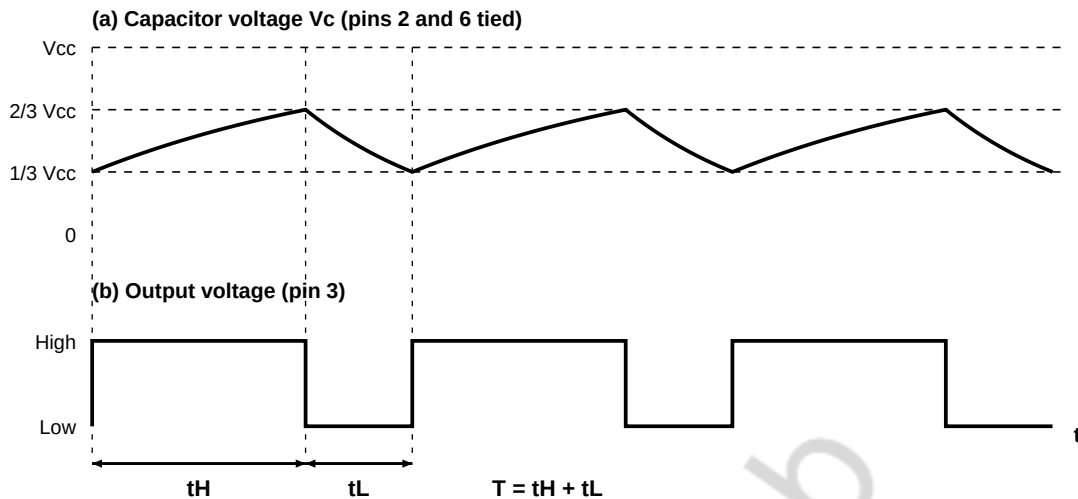


Fig. 6.8: Waveforms of the astable multivibrator ($R_1 = R_2$ shown)

The capacitor voltage therefore swings between $\frac{1}{3} V_{CC}$ and $\frac{2}{3} V_{CC}$. Using the exponential charging and discharging equations between these two levels, we get the following results.

Quantity	Expression
HIGH time (charging through $R_1 + R_2$)	$t_H = 0.693 (R_1 + R_2) C$
LOW time (discharging through R_2)	$t_L = 0.693 R_2 C$
Total period	$T = t_H + t_L = 0.693 (R_1 + 2 R_2) C$
Frequency	$f = 1 / T = 1.44 / [(R_1 + 2 R_2) C]$
Duty cycle	$D = t_H / T = (R_1 + R_2) / (R_1 + 2 R_2) (\times 100 \%)$

Remarks. Because the charging path ($R_1 + R_2$) is always longer than the discharging path (R_2), t_H is always greater than t_L and the duty cycle of the basic circuit is always **greater than 50 %**. It approaches 50 % when R_1 is made much smaller than R_2 . A duty cycle below 50 % (or close to exactly 50 %) is obtained by connecting a diode across R_2 , with its anode towards pin 7: the capacitor then charges through R_1 and the diode, bypassing R_2 , so that $t_H = 0.693 R_1 C$, $t_L = 0.693 R_2 C$ and $D = R_1 / (R_1 + R_2)$.

Worked Example 6.3

An astable 555 uses $R_1 = 1 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$ and $C = 0.1 \text{ }\mu\text{F}$. Find t_H , t_L , frequency and duty cycle.

$$t_H = 0.693 (1 \text{ k} + 10 \text{ k})(0.1 \text{ }\mu\text{F}) = 0.693 \times 11 \times 10^3 \times 10^{-7} = 0.762 \text{ ms}$$

$$t_L = 0.693 \times 10 \times 10^3 \times 10^{-7} = 0.693 \text{ ms}$$

$$T = 0.762 + 0.693 = 1.455 \text{ ms, so } f = 1 / T \approx \mathbf{687 \text{ Hz}}$$

$$D = t_H / T = 0.762 / 1.455 = 0.524, \text{ i.e. } \mathbf{52.4 \%}.$$

Worked Example 6.4

Design an astable 555 oscillator for $f = 1 \text{ kHz}$ with duty cycle 60 %. Take $C = 0.1 \mu\text{F}$.

Solution: $D = (R_1 + R_2) / (R_1 + 2 R_2) = 0.6$ gives $0.4 R_1 = 0.2 R_2$, i.e. $R_2 = 2 R_1$.

$T = 1 \text{ ms} = 0.693 (R_1 + 2 R_2) C = 0.693 \times 5 R_1 \times 10^{-7}$, so $R_1 = 10^{-3} / (3.465 \times 10^{-7}) \approx 2.9 \text{ k}\Omega$.

Hence $R_1 \approx 2.9 \text{ k}\Omega$ and $R_2 \approx 5.8 \text{ k}\Omega$ (use the nearest standard values or trimmer potentiometers).

Applications of astable mode:

- clock pulse generator for counters and digital circuits;
- LED flasher, alarm, siren and tone generator;
- pulse-width modulation and voltage-controlled oscillator (using pin 5);
- metronome, electronic buzzer and frequency source for testing.

6.3.3 Comparison of Monostable and Astable Modes

Point	Monostable mode	Astable mode
Stable states	One	None
External trigger	Required for each pulse	Not required (self-starting)
Output	Single pulse of width T	Continuous rectangular wave
Timing components	One R and one C	Two resistors (R_1, R_2) and one C
Main formula	$T = 1.1 RC$	$f = 1.44 / [(R_1 + 2 R_2) C]$
Pins 2 and 6	Pin 2 is the trigger input; pin 6 joined to pin 7	Pins 2 and 6 are joined together
Typical uses	Delay, pulse stretching, touch switch	Clock, flasher, siren, PWM

6.3.4 Practical Precautions

- always bypass pin 5 with a $0.01 \mu\text{F}$ capacitor and decouple the supply close to the IC;
- keep the reset pin 4 at V_{CC} when it is not used, otherwise noise may reset the timer;
- use stable (film or ceramic) capacitors where accuracy is needed; electrolytic capacitors leak and have wide tolerance;
- keep R_1 and R_2 above about $1 \text{ k}\Omega$ so that the discharge transistor current stays within limits;
- in monostable mode ensure that the trigger pulse is shorter than the output pulse.

Key Points of Section 6.3

- Monostable: $T = 1.1 RC$; trigger at pin 2; pins 6 and 7 joined to the R–C junction.
- Astable: $t_H = 0.693 (R_1 + R_2) C$, $t_L = 0.693 R_2 C$, $f = 1.44 / [(R_1 + 2 R_2) C]$.
- Capacitor voltage in astable mode swings between $\frac{1}{3} V_{CC}$ and $\frac{2}{3} V_{CC}$.
- Basic astable duty cycle is always above 50 %; a diode across R_2 reduces it.

6.4 Principle of Operation of Digital Timer

6.4.1 Introduction

An analog (RC) timer depends on the values of R and C, which drift with temperature, ageing and tolerance, and which become impractical for very long intervals. A **digital timer** removes these difficulties. It measures time by **counting the pulses of a stable clock**. If the clock frequency is f_{clk} (period $T_{clk} = 1 / f_{clk}$) and N pulses are counted, the elapsed time is

$$t = N \times T_{clk} = N / f_{clk}$$

The accuracy of the timer is therefore decided by the accuracy of the clock, and the resolution (smallest time step) is one clock period. The time can be set digitally and shown on a numeric display.

6.4.2 Block Diagram

Fig. 6.9 shows the main blocks of a digital timer.

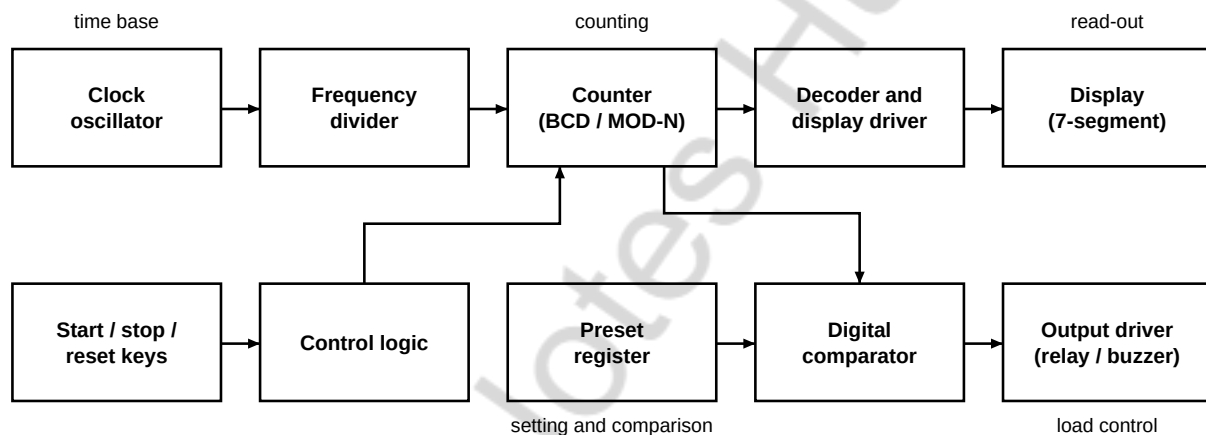


Fig. 6.9: Block diagram of a digital timer

6.4.3 Function of the Blocks

Block	Function	Typical implementation
Clock oscillator	Generates stable pulses that act as the time base.	Crystal oscillator (e.g. 32.768 kHz), 50 Hz mains-derived pulses in India, or a 555 astable circuit
Frequency divider	Divides the high clock frequency to a convenient rate such as 1 Hz or 10 Hz.	Chain of flip-flops; 15 stages divide 32.768 kHz ($2^{15} = 32768$) to exactly 1 Hz
Counter	Counts the pulses and holds the elapsed (or remaining) time in BCD or binary form.	Decade ($\div 10$) and MOD-6 counters for seconds and minutes; MOD-60 for 60 s / 60 min
Preset register and comparator	Stores the time set by the user and compares it with the counter content; gives a 'match' signal when they are equal.	Thumbwheel / push-button switches with registers and a digital comparator
Control logic	Handles the start, stop, reset and hold commands and gates the clock to the counter.	Gates and flip-flops, or a small controller
Decoder and display driver	Converts the BCD count into 7-segment code and drives the display.	BCD-to-7-segment decoder (e.g. 7447 / 7448)

Block	Function	Typical implementation
Display	Shows the time to the user.	7-segment LED or LCD
Output driver	Switches the load when the set time is reached.	Transistor / relay driver, buzzer

6.4.4 Principle of Operation

1. The required time is **set** in the preset register by switches or keys.
2. On a **start** command the control logic clears the counter and allows the clock pulses, after division, to reach it.
3. The counter **counts** the pulses once per time step (for example once per second) and the decoder and display show the elapsed time.
4. The digital comparator keeps comparing the counter content with the preset value.
5. When both are equal (match), the control logic **stops the count** and the output driver switches the load ON, OFF or sounds the buzzer. A reset command prepares the timer for the next operation.

A **count-down timer** works the other way round: the preset value is loaded into a down-counter, and the output is produced when the counter reaches zero, so that no comparator is needed.

6.4.5 Timer Functions Obtained with Digital Timers

Function	Behaviour of the output
ON-delay	Output turns ON a preset time after the start signal is applied.
OFF-delay	Output stays ON for the preset time after the start signal is removed.
Interval (one-shot)	Output is ON for the preset time only, then turns OFF automatically.
Repeat cycle (flasher)	Output switches ON and OFF repeatedly with set ON and OFF times.
Stopwatch (count-up)	Displays the elapsed time from zero until it is stopped.

6.4.6 Accuracy and Resolution

- **Resolution** equals one clock period T_{clk} . A 1 kHz clock gives 1 ms resolution; a 1 Hz clock gives 1 s resolution.
- **Accuracy** equals the clock accuracy. A quartz crystal is typically accurate to 20–50 ppm, which is about 4 s of error in a whole day for 50 ppm. A mains-derived 50 Hz clock is less accurate because the mains frequency varies slightly.
- **Range** is decided by the counter length. An n-bit counter can count up to 2^n pulses, so a longer counter gives a longer time without needing a larger capacitor.

Worked Example 6.5

A digital timer is driven by a 10 Hz clock. How many counts are required for a delay of 90 s?

Solution: $N = t \times f_{\text{clk}} = 90 \times 10 = \mathbf{900 \text{ counts}}$.

Worked Example 6.6

A 12-bit binary counter is clocked at 100 Hz. Find the resolution and the maximum time it can measure.

Solution: $T_{\text{clk}} = 1 / 100 = 10 \text{ ms}$ (resolution). Number of counts = $2^{12} = 4096$.

Maximum time = $4096 \times 10 \text{ ms} = \mathbf{40.96 \text{ s}}$.

6.4.7 Comparison of Analog (555) and Digital Timers

Point	Analog timer (RC / IC 555)	Digital timer
Timing element	Resistor and capacitor	Clock oscillator and counter
Accuracy	Moderate (a few percent); depends on R, C and temperature	High; decided by the crystal clock
Time range	Microseconds to minutes; long delays need large R and C	Milliseconds to days or more, by lengthening the counter
Setting of time	Potentiometer or fixed components; hard to read exactly	Exact numeric setting by switches or keys
Display	Usually none	Numeric display of set and elapsed time
Circuit complexity and cost	Very simple and cheap	More ICs, higher cost
Typical use	Simple delays, pulse and clock generation	Clocks, ovens, washing machines, industrial process timers

In practice the two are often combined: a 555 astable circuit is frequently used as the clock source for a digital counter. The 555 therefore remains useful even in digital timing systems.

6.4.8 Applications of Digital Timers

- digital clocks, stopwatches and countdown timers;
- microwave ovens, washing machines and other home appliances;
- traffic light controllers and industrial process sequencing;
- photographic exposure timers and parking meters;
- test and measuring instruments such as frequency counters and time-interval meters.

Key Points of Section 6.4

- Digital timer measures time by counting clock pulses: $t = N \times T_{\text{clk}}$.
- Main blocks: clock oscillator, frequency divider, counter, preset register and comparator, control logic, decoder / display and output driver.
- Accuracy comes from the crystal clock; range is set by the number of counter bits.
- $32.768 \text{ kHz} \div 2^{15} = 1 \text{ Hz}$ (15 flip-flops).

Chapter Summary and Formula Sheet

Electronic timers use the exponential charging of an RC network (analog) or the counting of clock pulses (digital) to create time intervals. The IC 555 combines a divider, two comparators, an SR flip-flop, a discharge transistor and an output stage, and with a few external parts it works as a monostable or astable multivibrator.

Topic	Formula / Value
Capacitor charging	$v_c = V_s (1 - e^{-t/RC})$; $\tau = RC$
Delay to threshold V_{th}	$t_d = RC \ln [V_s / (V_s - V_{th})]$
555 reference levels	Threshold: $\frac{2}{3} V_{CC}$; Trigger: $\frac{1}{3} V_{CC}$; with control voltage V_C : V_C and $V_C/2$
Monostable pulse width	$T = 1.1 RC$
Astable HIGH time	$t_H = 0.693 (R_1 + R_2) C$
Astable LOW time	$t_L = 0.693 R_2 C$
Astable period and frequency	$T = 0.693 (R_1 + 2 R_2) C$; $f = 1.44 / [(R_1 + 2 R_2) C]$
Astable duty cycle	$D = (R_1 + R_2) / (R_1 + 2 R_2)$
Digital timer	$t = N \times T_{clk} = N / f_{clk}$
n-bit counter	Maximum count = 2^n

Pin Quick Reference

1	2	3	4	5	6	7	8
GND	Trigger	Output	Reset	Control	Threshold	Discharge	V_{CC}

Multiple Choice Questions

Choose the correct answer. The answer key is given after the questions.

- Q1.** The three resistors in the internal voltage divider of the IC 555 each have a value of
- (a) 1 k Ω
 - (b) 10 k Ω
 - (c) 5 k Ω
 - (d) 100 k Ω
- Q2.** The threshold comparator of the 555 changes its output when the voltage at pin 6 exceeds
- (a) $V_{CC}/3$
 - (b) $V_{CC}/2$
 - (c) V_{CC}
 - (d) $2V_{CC}/3$
- Q3.** The trigger comparator of the 555 operates when the voltage at pin 2 falls below
- (a) $V_{CC}/3$
 - (b) $V_{CC}/2$
 - (c) $2V_{CC}/3$
 - (d) V_{CC}
- Q4.** The discharge pin of the IC 555 is pin number
- (a) 3
 - (b) 7
 - (c) 5
 - (d) 6
- Q5.** The pulse width of a 555 monostable multivibrator is given by
- (a) 0.693 RC
 - (b) 1.44 RC
 - (c) 1.1 RC
 - (d) 2.2 RC
- Q6.** The output frequency of a 555 astable multivibrator is
- (a) $1.1 / RC$
 - (b) $0.693 / [(R_1 + R_2) C]$
 - (c) $1 / 2RC$
 - (d) $1.44 / [(R_1 + 2R_2) C]$
- Q7.** The duty cycle of the basic 555 astable circuit (without a diode) is always
- (a) less than 50 %
 - (b) greater than 50 %
 - (c) exactly 50 %
 - (d) equal to 0 %

- Q8.** Pin 5 of the IC 555 is used as the
- (a) reset input
 - (b) output terminal
 - (c) control voltage input
 - (d) ground terminal
- Q9.** The reset pin (pin 4) of the 555 resets the timer when it is pulled
- (a) LOW
 - (b) HIGH
 - (c) to $2V_{CC}/3$
 - (d) to $V_{CC}/3$
- Q10.** The number of stable states of a monostable multivibrator is
- (a) zero
 - (b) two
 - (c) three
 - (d) one
- Q11.** After one time constant, a capacitor charging through a resistor reaches about
- (a) 63.2 % of the supply
 - (b) 36.8 % of the supply
 - (c) 50 % of the supply
 - (d) 100 % of the supply
- Q12.** In astable mode the voltage across the timing capacitor varies between
- (a) 0 and V_{CC}
 - (b) 0 and $V_{CC}/3$
 - (c) $V_{CC}/3$ and $2V_{CC}/3$
 - (d) $2V_{CC}/3$ and V_{CC}
- Q13.** A 32.768 kHz crystal oscillator followed by 15 flip-flop stages gives an output of
- (a) 1 kHz
 - (b) 1 Hz
 - (c) 50 Hz
 - (d) 10 Hz
- Q14.** If N clock pulses of period T_{clk} are counted, the time measured by a digital timer is
- (a) $N \times f_{clk}$
 - (b) $N \times T_{clk}$
 - (c) $N + T_{clk}$
 - (d) f_{clk} / N
- Q15.** In a digital timer, the block that converts the BCD count into 7-segment code is the
- (a) counter
 - (b) comparator
 - (c) frequency divider
 - (d) decoder / display driver

Answer Key

Q.No.	1	2	3	4	5	6	7	8
Answer	c	d	a	b	c	d	b	c

Q.No.	9	10	11	12	13	14	15	
Answer	a	d	a	c	b	b	d	

Poly Notes Hub

Broad Questions

Answer the following questions in detail. Draw neat diagrams wherever required.

- Q1.** Explain the principle of operation of an electronic timer with the help of a block diagram. Derive the expression for the delay time of an RC timing network when the comparator threshold is $\frac{2}{3}$ of the supply voltage.
- Q2.** Classify timers. Compare electromechanical, analog electronic and digital timers with respect to accuracy, range, cost and applications.
- Q3.** Draw the pin diagram of the IC 555 and explain the function of each pin. Mention the supply voltage range and the main features of the IC.
- Q4.** Draw the internal block diagram of the IC 555 and explain the function of the voltage divider, the two comparators, the flip-flop, the discharge transistor and the output stage.
- Q5.** Explain the role of the control voltage pin (pin 5) and the reset pin (pin 4). How are the threshold levels changed by an external control voltage?
- Q6.** With a neat circuit diagram and waveforms, explain the working of the IC 555 as a monostable multivibrator. Derive the expression $T = 1.1 RC$ for the pulse width and list four applications.
- Q7.** With a neat circuit diagram and waveforms, explain the working of the IC 555 as an astable multivibrator. Derive the expressions for t_H , t_L , frequency and duty cycle.
- Q8.** Solve: (a) A 555 monostable uses $R = 47 \text{ k}\Omega$ and $C = 10 \text{ }\mu\text{F}$; find the output pulse width. (b) Design a 555 astable circuit for a frequency of 500 Hz and a duty cycle of 60 % using $C = 0.1 \text{ }\mu\text{F}$. (c) For $R_1 = 4.7 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$ and $C = 0.01 \text{ }\mu\text{F}$, find t_H , t_L , f and the duty cycle.
- Q9.** Why is the duty cycle of the basic 555 astable circuit always greater than 50 %? Show how a diode can be used to obtain a duty cycle below 50 % and write the new expressions for t_H and t_L .
- Q10.** Explain the principle of operation of a digital timer with a block diagram. Describe the function of each block, and compare it with an analog timer built using the IC 555.

— End of Chapter 6: Timer Circuits —