
Electronics Devices & Circuits

Chapter 7

Elementary Idea of UJT and SCR

Topic 7.1 : Basic Construction and Operation of UJT and SCR

(Detailed Notes)

For Diploma / Degree Engineering Students

Part	Contents of these notes
A	Unijunction Transistor (UJT): introduction, construction, symbol, equivalent circuit, working, V-I characteristics, parameters, relaxation oscillator, applications
B	Silicon Controlled Rectifier (SCR): introduction, construction, symbol, working modes, two-transistor analogy, V-I characteristics, turn-on and turn-off methods, ratings, protection, applications
C	Comparison of UJT and SCR, quick revision table of key formulas
D	Practice section: 15 Multiple Choice Questions with answer key, and 10 broad questions

PART A : UNIJUNCTION TRANSISTOR (UJT)

7.1.1 Introduction to UJT

The **Unijunction Transistor (UJT)** is a three-terminal semiconductor switching device that contains only **one PN junction**. This single junction is the reason for the name *uni* (one) *junction*. Unlike an ordinary Bipolar Junction Transistor (BJT), which has two junctions and is mainly used for amplification, a UJT is **not used as an amplifier**. It is used as a **trigger, switch, and oscillator** device because it shows a special **negative resistance** property. Since it has one PN junction and two ohmic base contacts, it is also called a **double-base diode**.

Key points about UJT

- It is a three-terminal device: **Emitter (E)**, **Base-1 (B1)** and **Base-2 (B2)**.
- It has only one PN junction (between the emitter and the N-type bar).
- It works as a **voltage-controlled switch**: it remains OFF until the emitter voltage reaches a fixed **peak-point voltage (V_p)**, then it turns ON suddenly.
- It exhibits a **negative resistance region** in its emitter characteristic.
- Popular device types: **2N2646** and **2N2647**.

7.1.2 Construction of UJT

A UJT is built on a lightly doped **N-type silicon bar**. Two **ohmic (non-rectifying) contacts** are made at the two ends of the bar; these are the terminals **Base-1 (B1)** and **Base-2 (B2)**. On one side of the bar, a small heavily doped **P-type region** is formed by alloying or diffusion. This P-region forms the **emitter (E)** and creates a single PN junction with the N-type bar. The emitter is placed **closer to B2** than to B1, so that the resistance between the emitter junction and B1 is larger than the resistance between the emitter junction and B2.

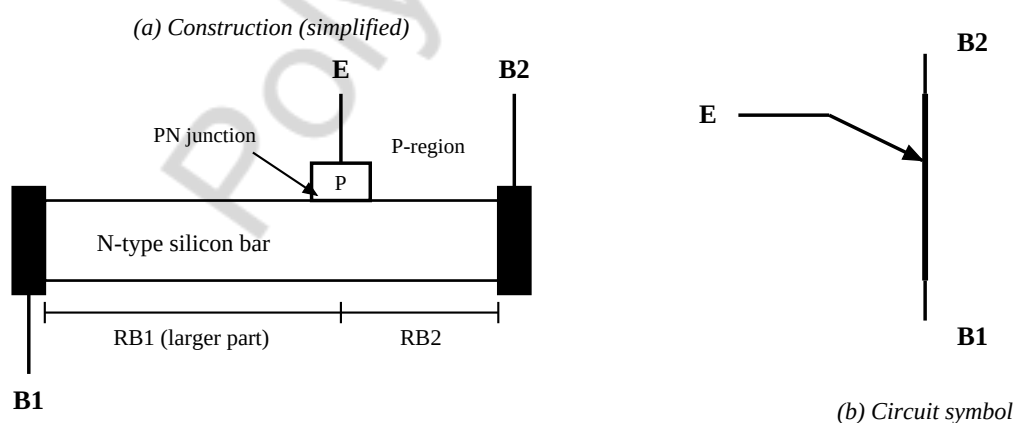


Fig. 7.1 : Construction and circuit symbol of a UJT

The N-type bar is **lightly doped**, so its resistance is high. The P-type emitter is **heavily doped** so that, when the junction is forward biased, a large number of holes are injected into the bar. The arrow in the symbol is drawn on the emitter and points **towards the bar**, showing the direction of conventional current when the junction is forward biased.

Terminals of UJT

Terminal	Symbol	Function
Emitter	E	P-type region; input terminal used to trigger the device with voltage V_E .
Base-1	B1	Lower end of the N-bar; connected to ground (negative) side. Output (pulse) is usually taken from B1.
Base-2	B2	Upper end of the N-bar; connected to positive supply V_{BB} through a resistor.

7.1.3 Equivalent Circuit of UJT

The N-type bar behaves like a resistance. The emitter junction divides this bar into two parts. Therefore the UJT can be represented by two resistances in series, R_{B1} and R_{B2} , with a diode connected from the emitter to the junction point A between them. The total resistance of the bar (with the emitter open) is called the **interbase resistance** R_{BB} .

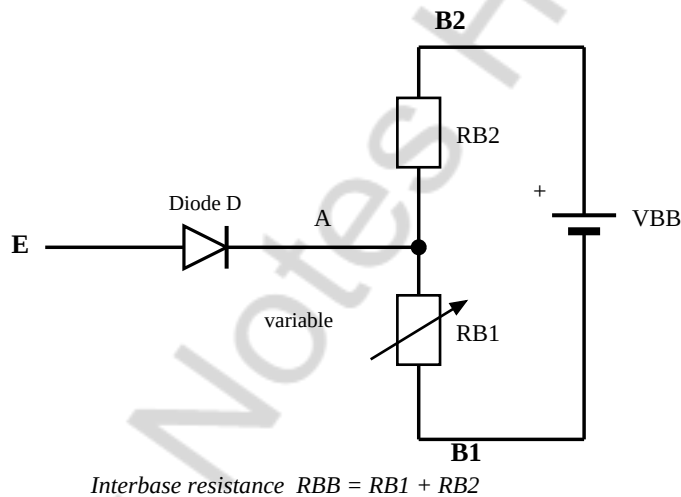


Fig. 7.2 : Equivalent circuit of UJT

$$R_{BB} = R_{B1} + R_{B2}$$

The resistance R_{B1} is **variable**: when the emitter injects holes into the bar, the conductivity of the B1 region increases and R_{B1} falls. This effect is called **conductivity modulation**. R_{B2} is almost constant. The ratio of R_{B1} to R_{BB} is known as the **intrinsic stand-off ratio** (η).

$$\eta = R_{B1} / (R_{B1} + R_{B2}) = R_{B1} / R_{BB}$$

With the emitter open and a supply V_{BB} applied between B2 and B1, the voltage across R_{B1} (at point A) is given by the potential divider rule:

$$V_A = [R_{B1} / (R_{B1} + R_{B2})] V_{BB} = \eta V_{BB}$$

The emitter diode starts conducting only when V_E exceeds V_A by the diode drop V_D (about 0.5 V to 0.7 V for silicon). Hence the **peak-point voltage** is:

$$V_P = \eta V_{BB} + V_D$$

The value of η depends on the construction of the device and is typically between **0.5 and 0.8**. For example, for the 2N2646 it lies roughly between 0.56 and 0.75.

7.1.4 Working (Operation) of UJT

For normal operation, a positive voltage V_{BB} is applied to B2 with respect to B1, and a variable positive voltage V_E is applied to the emitter with respect to B1. The operation is explained in the following stages.

- 1 **Cut-off stage ($V_E < V_p$):** The voltage at point A is ηV_{BB} . When V_E is less than $\eta V_{BB} + V_D$, the emitter PN junction is **reverse biased**. Only a very small leakage current flows in the emitter. The UJT is in the OFF state with a very high emitter-to-B1 resistance.
- 2 **Triggering ($V_E = V_p$):** When V_E reaches V_p , the junction becomes **forward biased**. Holes are injected from the P-type emitter into the N-type bar. Because B1 is at a lower potential, these holes are swept towards B1.
- 3 **Regenerative action:** The injected holes increase the conductivity of the region between the emitter and B1. R_{B1} drops sharply, so the voltage V_A falls. A lower V_A means more forward bias on the junction, hence more hole injection and still lower R_{B1} . This is a **cumulative (regenerative) process** that turns the device ON very quickly.
- 4 **Negative resistance region:** During this process, the emitter current I_E **increases** while the emitter voltage V_E **decreases**. This is the negative resistance region.
- 5 **Saturation stage:** After the valley point (V_V, I_V), the bar is saturated with holes, R_{B1} reaches its minimum value and the device behaves like a forward-biased diode in series with a small resistance. V_E now rises slowly with I_E .
- 6 **Turn-off:** The UJT returns to the OFF state when the emitter current is reduced below the valley current I_V (or V_E falls below V_V), because the injection of holes stops and R_{B1} returns to its high value.

7.1.5 V-I (Emitter) Characteristics of UJT

The emitter characteristic is a plot of the **emitter voltage V_E** against the **emitter current I_E** for a fixed interbase voltage V_{BB} . It has three distinct regions.

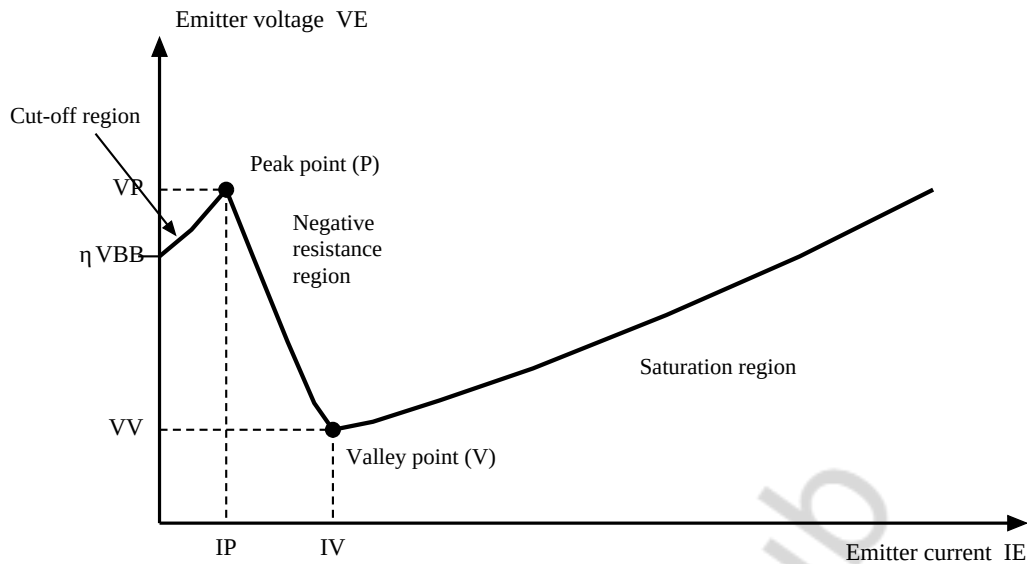


Fig. 7.3 : Emitter characteristic of UJT (V_E versus I_E)

Region	Condition	Behaviour
Cut-off region	$V_E < V_P$	Emitter junction reverse biased; I_E is only a small leakage current; device is OFF.
Negative resistance region	Between peak point P and valley point V	I_E rises while V_E falls; resistance between E and B1 is negative; device switches rapidly.
Saturation region	Beyond valley point V	R_{B1} is minimum; device is fully ON; V_E increases slowly with I_E like a forward diode.

Important points on the characteristic

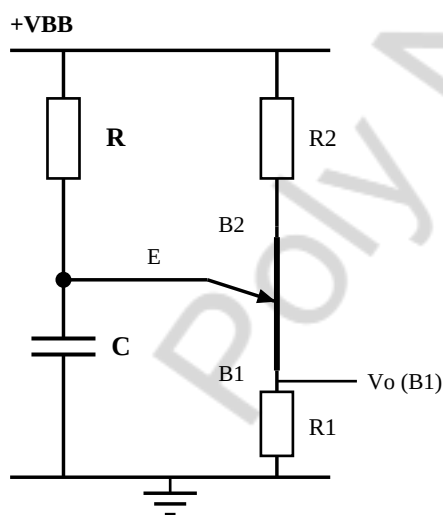
- **Peak point (V_P, I_P):** the point where the emitter junction just becomes forward biased and the negative resistance region begins. I_P is very small (in microamperes).
- **Valley point (V_V, I_V):** the point where the negative resistance region ends and saturation begins. V_V is much lower than V_P .
- A larger V_{BB} gives a larger V_P (because $V_P = \eta V_{BB} + V_D$), so the characteristic shifts upward as V_{BB} increases.

7.1.6 Important Parameters of UJT

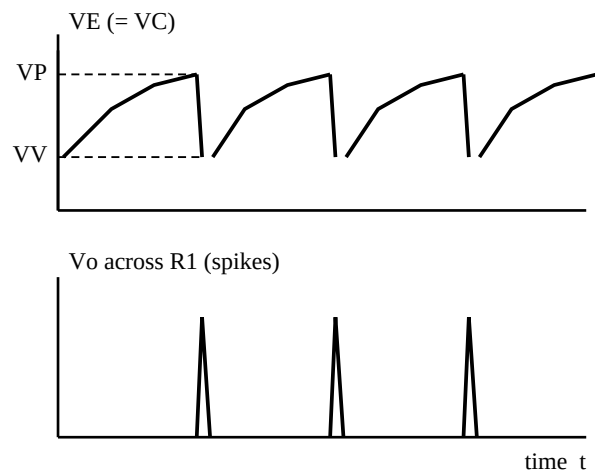
Parameter	Meaning	Typical idea
Intrinsic stand-off ratio (η)	R_{B1} / R_{BB} ; fixes the triggering voltage	0.5 to 0.8
Interbase resistance (R_{BB})	Resistance between B1 and B2 with emitter open	A few $k\Omega$ (about 4 to 10 $k\Omega$)
Peak-point voltage (V_P)	Emitter voltage at which UJT fires	$V_P = \eta V_{BB} + V_D$
Peak-point current (I_P)	Minimum emitter current needed to fire the UJT	Microamperes
Valley-point voltage (V_V)	Emitter voltage at the valley point	Low (a few volts)
Valley-point current (I_V)	Emitter current at the valley point; below it UJT turns OFF	Milliamperes
Emitter reverse leakage (I_{EO})	Leakage current when emitter junction is reverse biased	Very small

7.1.7 UJT Relaxation Oscillator

The most important application of a UJT is the **relaxation oscillator**, which generates a sawtooth wave and a train of sharp pulses. In the circuit, the capacitor C is charged from V_{BB} through the resistor R . Resistors R_1 (in series with B1) and R_2 (in series with B2) are small; R_2 also gives temperature compensation.



(a) UJT relaxation oscillator



(b) Output waveforms

Fig. 7.4 : UJT relaxation oscillator and its output waveforms

Working of the oscillator

- 1 When the supply is switched ON, the capacitor C charges exponentially through R towards V_{BB} . The UJT is OFF because $V_E (= V_C)$ is below V_P .
- 2 When V_C reaches V_P , the emitter junction becomes forward biased and the UJT **fires**. R_{B1} drops suddenly.
- 3 The capacitor discharges rapidly through the low-resistance path E-B1 and R_1 . A sharp **positive spike** appears across R_1 .
- 4 When V_C falls to the valley voltage V_V , the emitter current drops below I_V and the UJT turns OFF.
- 5 The capacitor starts charging again, and the cycle repeats. The result is a **sawtooth wave** at the emitter and **narrow pulses** at B1 (positive spikes) and B2 (small negative spikes).

Neglecting the small valley voltage, the time period and the frequency of oscillation are:

$$T = R C \ln [1 / (1 - \eta)] \text{ and } f = 1 / T = 1 / \{ R C \ln [1 / (1 - \eta)] \}$$

If η is about 0.63, then $\ln[1/(1 - \eta)]$ is approximately 1, so $f \sim 1 / (RC)$.

Condition for proper oscillation: the resistance R must be chosen so that the UJT can fire and can also turn OFF:

$$(V_{BB} - V_V) / I_V < R < (V_{BB} - V_P) / I_P$$

If R is too large, the charging current is below I_P and the UJT never fires. If R is too small, the current stays above I_V and the UJT cannot turn OFF.

Solved examples

Problem	Solution
A UJT has $V_{BB} = 20 \text{ V}$, $\eta = 0.6$ and $V_D = 0.6 \text{ V}$. Find V_P .	$V_P = \eta V_{BB} + V_D = (0.6 \times 20) + 0.6 = 12 + 0.6 = \mathbf{12.6 \text{ V}}$
In a UJT oscillator $R = 100 \text{ k}\Omega$, $C = 0.01 \text{ }\mu\text{F}$ and $\eta = 0.63$. Find the frequency.	$T = RC \ln[1/(1 - 0.63)] = 100 \times 10^3 \times 0.01 \times 10^{-6} \times \ln(2.7) = 10^{-3} \times 1 = 1 \text{ ms}$. So $f = 1/T = \mathbf{1 \text{ kHz}}$ (approx.)
A UJT has $R_{B1} = 3 \text{ k}\Omega$ and $R_{B2} = 2 \text{ k}\Omega$. Find η and R_{BB} .	$R_{BB} = 3 + 2 = \mathbf{5 \text{ k}\Omega}$; $\eta = 3/5 = \mathbf{0.6}$

7.1.8 Applications, Advantages and Limitations of UJT

Applications	Advantages	Limitations
<ul style="list-style-type: none">• Relaxation (sawtooth / pulse) oscillators• Triggering of SCR and TRIAC• Timing and delay circuits• Phase-control circuits• Voltage-sensing circuits• Pulse and sweep generators	<ul style="list-style-type: none">• Simple, low-cost circuits• Stable triggering voltage• Low power consumption• Good temperature stability• High pulse-current capability• Few components needed	<ul style="list-style-type: none">• Cannot be used as an amplifier• Low power-handling capacity• Limited to trigger / oscillator use• Frequency limited by C charging time• Parameters vary from device to device

7.1.9 Comparison : UJT and BJT

Basis	UJT	BJT
Number of PN junctions	One	Two
Terminals	Emitter, Base-1, Base-2	Emitter, Base, Collector
Main use	Switching, triggering, oscillators	Amplification and switching
Negative resistance	Present in emitter characteristic	Not present
Current carriers	Mainly majority carriers; holes injected	Both electrons and holes (bipolar)
Amplification	Cannot amplify	Can amplify

PART B : SILICON CONTROLLED RECTIFIER (SCR)

7.1.10 Introduction to SCR

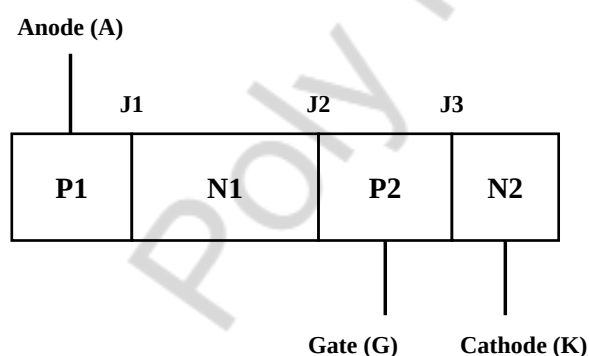
The **Silicon Controlled Rectifier (SCR)** is a **four-layer (PNPN)**, **three-terminal**, **three-junction** semiconductor device. It belongs to the **thyristor family** (other members are the TRIAC, DIAC and GTO). It acts as a **controllable, unidirectional switch**: it can be turned ON by a small gate current, it conducts current in **one direction only** (anode to cathode), and once ON, it stays ON even after the gate signal is removed. Because of this **latching** property, SCRs are widely used for controlling large amounts of power.

Key points about SCR

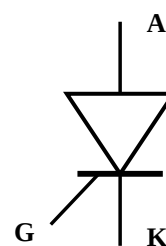
- Terminals: **Anode (A)**, **Cathode (K)** and **Gate (G)**.
- Four layers P-N-P-N and three junctions J_1, J_2, J_3 .
- Also called a **reverse-blocking triode thyristor**.
- Works like a rectifier whose conduction can be **controlled** by the gate.
- Handles high voltage and high current with a very small ON-state voltage drop (about 1 V to 1.5 V).

7.1.11 Construction of SCR

An SCR is made from a silicon wafer with four alternate layers of P-type and N-type material: $P_1-N_1-P_2-N_2$. The outer P-layer (P_1) is connected to the **anode**, the outer N-layer (N_2) is connected to the **cathode**, and the **gate** is connected to the inner P-layer (P_2) near the cathode. The three PN junctions formed are J_1 (P_1-N_1), J_2 (N_1-P_2) and J_3 (P_2-N_2).



(a) Four-layer PNPN structure



(b) Circuit symbol

Fig. 7.5 : Structure and circuit symbol of SCR

Layer	Doping	Role
P ₁ (anode layer)	Heavily doped	Connected to anode; injects holes into N ₁ .
N ₁ (N-base)	Lightly doped, thick	Determines the forward and reverse blocking voltage of the SCR.
P ₂ (gate layer)	Moderately doped, thin	Gate is attached here; controls the turn-ON of the SCR.
N ₂ (cathode layer)	Heavily doped	Connected to cathode; emits electrons into P ₂ .

High-power SCRs are mounted in **stud-type or press-pack** metal cases and fixed on a **heat sink**, because the power dissipated in the device must be removed to avoid overheating. The cathode lead is usually thinner, with a separate thin gate lead.

Terminals of SCR

Terminal	Symbol	Function
Anode	A	Positive terminal of the main circuit; load current enters here.
Cathode	K	Negative terminal of the main circuit; load current leaves here; reference for gate signal.
Gate	G	Control terminal; a small positive current pulse here turns the SCR ON.

7.1.12 Operation of SCR (Modes of Operation)

The behaviour of an SCR depends on the polarity of the voltage V_{AK} between anode and cathode and on the gate condition. There are **three modes** of operation.

(i) Reverse blocking mode (OFF state)

The anode is made **negative** with respect to the cathode. Junctions J₁ and J₃ become **reverse biased** and J₂ is forward biased. Only a very small **reverse leakage current** flows, so the SCR behaves like an open switch. If the reverse voltage is increased beyond the **reverse breakdown voltage (V_{BR})**, avalanche breakdown occurs and the device may be damaged by excess current.

(ii) Forward blocking mode (OFF state)

The anode is made **positive** with respect to the cathode, but the gate is open (or no gate current is given). Now J₁ and J₃ are forward biased, while the middle junction J₂ is **reverse biased**. Only a small **forward leakage current** flows, and the SCR is still OFF. If V_{AK} is increased up to the **forward breakover voltage (V_{BO})**, J₂ breaks down by avalanche and the SCR turns ON. This is not the normal way to turn ON an SCR.

(iii) Forward conduction mode (ON state)

The SCR is turned ON either by exceeding V_{BO} or, normally, by applying a small **positive gate current** while the anode is positive. The gate current injects carriers across J_3 and triggers a regenerative action: all three junctions become forward biased and the device conducts like a closed switch. The voltage drop across it falls to about 1 V to 1.5 V and the anode current is limited only by the external load. Once the anode current exceeds the **latching current (I_L)**, the gate loses control, and the SCR stays ON even if the gate signal is removed.

7.1.13 Two-Transistor Analogy of SCR

The regenerative turn-ON action of the SCR is easily understood by splitting the four-layer device into two interconnected transistors: a **PNP transistor Q_1 ($P_1-N_1-P_2$)** and an **NPN transistor Q_2 ($N_1-P_2-N_2$)**. The middle layers N_1 and P_2 are common to both transistors.

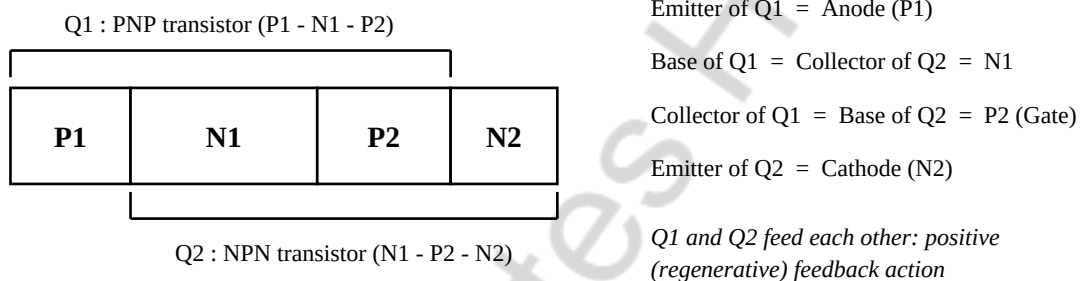


Fig. 7.6 : Two-transistor analogy of SCR

The collector current of Q_1 is the base current of Q_2 , and the collector current of Q_2 is the base current of Q_1 . Let α_1 and α_2 be the common-base current gains and I_{CBO1} , I_{CBO2} the leakage currents of the two transistors. Then:

$$I_{C1} = \alpha_1 I_A + I_{CBO1}, I_{C2} = \alpha_2 I_K + I_{CBO2}, I_K = I_A + I_G, I_A = I_{C1} + I_{C2}$$

Solving these equations gives the anode current:

$$I_A = [\alpha_2 I_G + I_{CBO1} + I_{CBO2}] / [1 - (\alpha_1 + \alpha_2)]$$

- At low currents, $\alpha_1 + \alpha_2$ is much less than 1, so I_A is small (only leakage): SCR is **OFF**.
- When a gate current I_G is applied, the emitter currents increase, α increases with current, and the sum $(\alpha_1 + \alpha_2)$ **approaches unity**.
- As $(\alpha_1 + \alpha_2) \rightarrow 1$, the denominator tends to zero and I_A rises rapidly (limited only by the external circuit): the SCR turns **ON** by regenerative feedback.

7.1.14 V-I Characteristics of SCR

The V-I characteristic is a plot of the anode current I_A against the anode-to-cathode voltage V_{AK} . It has a forward region (first quadrant) and a reverse region (third quadrant).

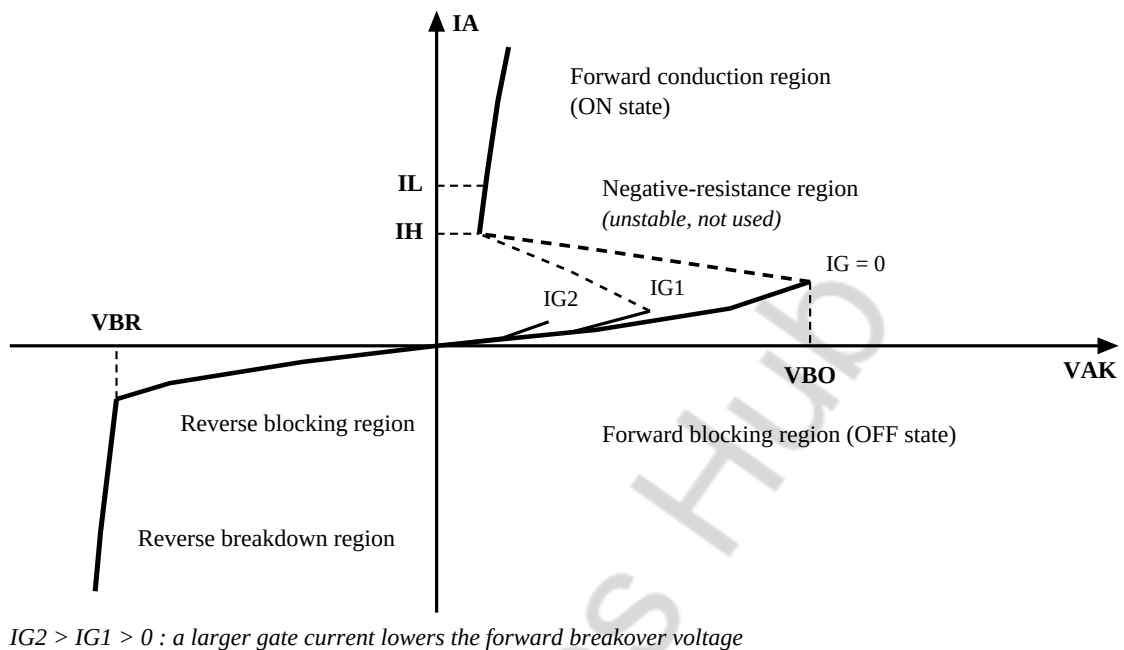


Fig. 7.7 : V-I characteristics of SCR

Region	Description
Reverse blocking region	V_{AK} negative; only a small reverse leakage current flows; SCR is OFF.
Reverse breakdown region	At V_{BR} the reverse current rises sharply (avalanche); the SCR may be damaged.
Forward blocking region	V_{AK} positive, gate open; small forward leakage current; SCR is OFF until V_{BO} is reached.
Negative-resistance region	Transition after breakover; voltage falls while current rises; unstable, passed through quickly.
Forward conduction region	SCR is ON; low voltage drop (about 1 V to 1.5 V); current is determined by the load.

With a larger gate current (I_{G1} , I_{G2}), the forward breakover voltage **decreases**. With a sufficient gate current, the SCR turns ON at a very low forward voltage, like an ordinary diode. This is the principle of **gate-controlled** turn-ON.

Latching current and holding current

Basis	Latching current (I_L)	Holding current (I_H)
Definition	Minimum anode current required to keep the SCR ON immediately after the gate signal is removed.	Minimum anode current required to keep the SCR ON once it is already conducting.
Applies to	Turn-ON process (just after triggering).	Steady ON-state; if I_A falls below I_H , SCR turns OFF.
Relative value	Higher (I_L is about 2 to 3 times I_H).	Lower.

7.1.15 Methods of Turning ON an SCR (Triggering)

Method	Explanation
Forward voltage (breakover) triggering	V_{AK} is raised to V_{BO} ; J_2 breaks down. Not recommended; may damage the SCR.
Gate triggering	A small positive gate current pulse is applied while the anode is positive. The most common and controllable method .
dv/dt triggering	A very rapid rise of anode voltage causes a charging current through the junction capacitance of J_2 , which can turn the SCR ON unintentionally.
Thermal (temperature) triggering	A rise in junction temperature increases leakage current; at high temperature the SCR can turn ON.
Light triggering	Light falling on the silicon creates electron-hole pairs that trigger the device (Light Activated SCR, LASCR).

7.1.16 Methods of Turning OFF an SCR (Commutation)

Once the SCR is ON, the gate cannot turn it OFF. To turn it OFF, the anode current must be reduced below the holding current I_H and the SCR must then be kept reverse biased for a short time (the **turn-off time** t_q , typically tens of microseconds) so that it regains its forward blocking ability. This process is called **commutation**.

- **Natural (line) commutation:** In AC circuits, the anode current naturally falls to zero at the end of every positive half cycle and the SCR turns OFF by itself.
- **Forced commutation:** In DC circuits there is no natural zero crossing, so extra circuits (a charged capacitor, an LC circuit, or an auxiliary SCR) are used to force the current to zero or to apply a reverse voltage.
- **Current interruption:** Opening a series switch or short-circuiting the SCR with a parallel switch reduces the current below I_H .

7.1.17 Important Ratings of SCR

Rating	Meaning
V_{DRM}	Repetitive peak forward off-state voltage that the SCR can block.
V_{RRM}	Repetitive peak reverse voltage that the SCR can withstand.
$I_{\text{T(av)}} / I_{\text{T(rms)}}$	Average / RMS ON-state current rating.
I_{TSM}	Surge (non-repetitive) peak current rating for a short duration.
$I_{\text{GT}}, V_{\text{GT}}$	Minimum gate current and gate voltage required to trigger the SCR.
$I_{\text{H}}, I_{\text{L}}$	Holding current and latching current.
dv/dt	Maximum rate of rise of anode voltage without false triggering.
di/dt	Maximum rate of rise of anode current that the SCR can tolerate at turn-ON without damage.
t_q	Circuit-commutated turn-off time.

7.1.18 Protection of SCR

- **dv/dt protection:** An **RC snubber circuit** connected across the SCR limits the rate of rise of voltage.
- **di/dt protection:** A small **series inductor** limits the rate of rise of current at turn-ON.
- **Over-current protection:** Fast-acting **fuses** and circuit breakers in the supply line.
- **Over-voltage protection:** Voltage-suppressing devices (such as varistors) and RC snubbers across the supply or the SCR.
- **Thermal protection:** Proper **heat sinks** and cooling (natural air, forced air or liquid) to limit the junction temperature.
- **Gate protection:** A series resistor or diode in the gate circuit to prevent excessive gate current or reverse gate voltage.

7.1.19 SCR as a Half-Wave Controlled Rectifier

When an SCR is connected in series with a load across an AC supply, it conducts only during the positive half cycle, and only after the gate pulse arrives. The angle of the supply voltage at which the SCR is triggered is called the **firing (delay) angle α** . By changing α , the average output voltage can be varied. For a resistive load with a supply of peak value V_m :

$$V_{dc} = (V_m / 2\pi) (1 + \cos \alpha)$$

For $\alpha = 0$ the SCR behaves like a normal diode rectifier, and as α increases the output voltage decreases. A UJT relaxation oscillator is often used to produce the gate pulses with an adjustable delay.

7.1.20 Applications, Advantages and Limitations of SCR

Applications	Advantages	Limitations
<ul style="list-style-type: none">• Controlled rectifiers (AC to DC)• Inverters and choppers• DC and AC motor speed control• Light dimmers and heater control• Battery chargers• Static switches and UPS• Crowbar over-voltage protection	<ul style="list-style-type: none">• Handles high voltage and current• Small gate power controls large load power• Very fast switching• No moving parts; silent• High efficiency (low ON-state drop)• Long life and small size	<ul style="list-style-type: none">• Gate loses control after turn-ON• Needs commutation circuit in DC• Conducts in one direction only• Sensitive to dv/dt and di/dt• Needs heat sink and protection• Generates harmonics in AC lines

PART C : COMPARISON AND QUICK REVISION

7.1.21 Comparison : UJT and SCR

Basis	UJT	SCR
Full form	Unijunction Transistor	Silicon Controlled Rectifier
Number of layers / junctions	Bar of N-type with one P-region; one PN junction	Four layers (PNPN); three junctions
Terminals	Emitter, Base-1, Base-2	Anode, Cathode, Gate
Family	Transistor-type switching device	Thyristor family
Special property	Negative resistance in emitter characteristic	Regenerative latching; unidirectional controlled conduction
Power handling	Low power	High power (high voltage and current)
Control	Triggered by emitter voltage reaching V_P	Triggered by gate current (or V_{BO})
Turn-off	Turns OFF when I_E falls below I_V	Turns OFF when I_A falls below I_H (commutation)
Main use	Triggering and oscillator circuits	Power control: rectifiers, inverters, motor control

7.1.22 Quick Revision : Key Formulas and Facts

Item	Formula / Fact
Interbase resistance	$R_{BB} = R_{B1} + R_{B2}$
Intrinsic stand-off ratio	$\eta = R_{B1} / (R_{B1} + R_{B2})$
Peak-point voltage of UJT	$V_P = \eta V_{BB} + V_D$
UJT oscillator frequency	$f = 1 / \{ R C \ln [1 / (1 - \eta)] \}$
Range of R in oscillator	$(V_{BB} - V_V)/I_V < R < (V_{BB} - V_P)/I_P$
SCR anode current (two-transistor)	$I_A = (\alpha_2 I_G + I_{CBO1} + I_{CBO2}) / [1 - (\alpha_1 + \alpha_2)]$
SCR turns ON when	$\alpha_1 + \alpha_2$ approaches 1
SCR turns OFF when	$I_A < I_H$ (and reverse bias applied for t_q)
Half-wave controlled rectifier	$V_{dc} = (V_m / 2\pi)(1 + \cos \alpha)$
Latching vs holding	$I_L > I_H$

PART D : PRACTICE QUESTIONS

Multiple Choice Questions (15 MCQs)

Choose the correct option for each question. The answer key is given at the end of this section.

Q1. The number of PN junctions present in a UJT is:

- (A) 2 (B) 1 (C) 3 (D) 0

Q2. The intrinsic stand-off ratio (η) of a UJT is given by:

- (A) $R_{B2} / (R_{B1} + R_{B2})$ (B) $R_{B1} \times R_{B2}$ (C) $(R_{B1} + R_{B2}) / R_{B1}$ (D) $R_{B1} / (R_{B1} + R_{B2})$

Q3. The peak-point voltage of a UJT is:

- (A) ηV_{BB} (B) $\eta V_{BB} + V_D$ (C) $V_{BB} - V_D$ (D) V_{BB} / η

Q4. The negative resistance region of a UJT lies between:

- (A) Origin and peak point (B) Valley point and saturation region (C) Peak point and valley point (D) Reverse breakdown and peak point

Q5. The approximate frequency of a UJT relaxation oscillator is:

- (A) $1 / \{ RC \ln[1 / (1 - \eta)] \}$ (B) $1 / (2\pi RC)$ (C) $1 / (RC \ln \eta)$ (D) $RC / \ln(1 - \eta)$

Q6. An SCR has _____ layers and _____ junctions:

- (A) 3 layers, 2 junctions (B) 4 layers, 4 junctions (C) 4 layers, 2 junctions (D) 4 layers, 3 junctions

Q7. In an SCR, the gate terminal is connected to the:

- (A) N-layer near the anode (B) P-layer near the anode (C) P-layer near the cathode (D) N-layer near the cathode

Q8. The minimum anode current below which an SCR that is already conducting turns OFF is called:

- (A) Holding current (B) Latching current (C) Leakage current (D) Breakover current

Q9. An SCR that is conducting can be turned OFF by:

- (A) Applying a negative gate pulse (B) Reducing the anode current below the holding current (C) Increasing the gate current (D) Increasing the anode voltage

Q10. Turning ON an SCR due to a very rapid rise of anode voltage is called:

- (A) di/dt triggering (B) Thermal triggering (C) dv/dt triggering (D) Light triggering

Q11. Which of the following is NOT a method of turning ON an SCR?

- (A) Gate triggering (B) Light triggering (C) Thermal triggering (D) Reducing anode current below holding current

Q12. An RC snubber circuit connected across an SCR protects it against:

- (A) High dv/dt (B) High di/dt (C) Reverse gate voltage (D) Excessive gate current

Q13. The two-transistor analogy of an SCR consists of:

- (A) Two PNP transistors (B) One PNP and one NPN (C) Two NPN transistors (D) One UJT and one BJT transistor connected in regenerative feedback

Q14. In the two-transistor model, the SCR turns ON when the sum ($\alpha_1 + \alpha_2$):

- (A) is much less than 1 (B) is equal to 0 (C) is equal to 0.2 (D) approaches unity (1)

Q15. Which device is commonly used to generate trigger pulses for an SCR?

- (A) Zener diode (B) LED (C) UJT (D) LDR

Answer Key

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
B	D	B	C	A	D	C	A

Q9	Q10	Q11	Q12	Q13	Q14	Q15
B	C	D	A	B	D	C

Short Explanations

Q.	Ans.	Reason
1	B	A UJT has only one PN junction (emitter and N-bar).
2	D	$\eta = R_{B1} / R_{BB}$.
3	B	The emitter diode must overcome ηV_{BB} plus its own drop V_D .
4	C	I_E rises while V_E falls between P and V.
5	A	$T = RC \ln[1/(1 - \eta)]$, so f is its reciprocal.
6	D	SCR = P-N-P-N: four layers with junctions J_1, J_2, J_3 .
7	C	The gate is taken from the P_2 layer next to the cathode.
8	A	Holding current is the minimum current to remain in the ON state.
9	B	Gate has no control after turn-ON; the anode current must fall below I_H .
10	C	A fast-rising anode voltage drives a charging current through J_2 capacitance.
11	D	Reducing anode current below I_H is a turn-OFF method, not a turn-ON method.
12	A	The snubber limits dv/dt ; a series inductor limits di/dt .
13	B	Q_1 (PNP) and Q_2 (NPN) are cross-coupled.
14	D	As the sum nears 1, the denominator of the I_A equation tends to zero.
15	C	A UJT relaxation oscillator provides sharp pulses for gating an SCR.

Broad Questions (10 Questions)

Write detailed answers with neat labelled diagrams wherever required.

- 1 Explain the construction of a Unijunction Transistor (UJT) with a neat diagram. Draw and explain its circuit symbol and the function of each terminal.
- 2 Draw the equivalent circuit of a UJT. Define interbase resistance and intrinsic stand-off ratio, and derive the expression for the peak-point voltage $V_p = \eta V_{BB} + V_D$.
- 3 Explain the working of a UJT with the help of its equivalent circuit. Discuss the cut-off, negative resistance and saturation regions.
- 4 Draw and explain the emitter (V_E versus I_E) characteristics of a UJT. Define peak point and valley point.
- 5 With a neat circuit diagram and waveforms, explain the working of a UJT relaxation oscillator. Derive the expression for its frequency and state the condition for the choice of R .
- 6 Explain the construction of an SCR with a neat diagram of its four-layer structure. Draw its symbol and state the function of anode, cathode and gate.
- 7 Explain the three modes of operation of an SCR: reverse blocking, forward blocking and forward conduction. Mention the state of the junctions in each mode.
- 8 Explain the two-transistor analogy of an SCR and derive the expression for the anode current I_A . Explain how regenerative action turns the SCR ON.
- 9 Draw and explain the V-I characteristics of an SCR. Define breakover voltage, latching current and holding current, and show the effect of gate current on the characteristic.
- 10 Describe the different methods of turning ON and turning OFF an SCR. Also explain the protection of an SCR against dv/dt and di/dt , and write any four applications of SCR.

- End of Notes -