DIPLOMA / ENGINEERING STUDY NOTES

ELECTRONICS DEVICES & CIRCUITS

Chapter 3

FIELD EFFECT TRANSISTOR

Topics Covered

3.1 Construction, operation and V-I characteristics of JFET, pinch-off voltage, drain resistance, transconductance, amplification factor and their relationship

3.2 Enhancement and depletion type MOSFET – concepts of CMOS

3.3 Differences between BJT and JFET

Extra: 15 Multiple Choice Questions with Answer Key and 10 Descriptive Questions

Notes in paragraph, list and table format with diagrams, designed for engineering students.

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3.1 Junction Field Effect Transistor (JFET)

3.1.0 Introduction to Field Effect Transistors

The **Field Effect Transistor (FET)** is a three-terminal semiconductor device in which the output (drain) current is controlled by an **electric field** set up by the input voltage. Unlike the Bipolar Junction Transistor (BJT), where both electrons and holes take part in conduction, a FET conducts through **only one type of charge carrier** (majority carriers) flowing through a semiconductor path called the **channel**. For this reason a FET is called a **unipolar device**. Since the control is exerted by a voltage and almost no input current flows, a FET is also called a **voltage-controlled device**.

Terminals of a FET

Terminal	Symbol	Function
Source	S	The terminal through which majority carriers enter the channel. Source current is I_S.
Drain	D	The terminal through which majority carriers leave the channel. Drain current is I_D. In a FET, $I_D = I_S$ because gate current is negligible.
Gate	G	The control terminal. The voltage applied here controls the width (conductivity) of the channel.
Channel	–	The semiconductor path between source and drain. It may be n-type or p-type.

Classification of FETs

Main type	Sub-type	Channel variants
JFET (Junction FET)	–	n-channel JFET, p-channel JFET
MOSFET (Metal Oxide Semiconductor FET), also called IGFET (Insulated Gate FET)	Depletion type (D-MOSFET)	n-channel, p-channel
	Enhancement type (E-MOSFET)	n-channel, p-channel

General features of FETs

- Voltage-controlled, unipolar device – conduction by majority carriers only.
- Very high input impedance (JFET: 10^8 Ω or more; MOSFET: 10^{10} to 10^{15} Ω).
- Low noise, because there are no minority-carrier injection and recombination effects.
- Better thermal stability – no thermal runaway.
- Occupies very small space, hence suitable for Large Scale Integration (LSI/VLSI).
- Gain-bandwidth product is lower than that of a BJT.

3.1.1 Construction of JFET

A JFET is basically a **bar of lightly doped semiconductor** (n-type or p-type) with ohmic contacts at both ends. In an **n-channel JFET**, the bar is n-type silicon. On the two opposite sides of the bar, heavily doped **p^+ regions** are formed by diffusion. These two p^+ regions are joined internally and brought out as a single terminal called the **gate**. The two p-n junctions formed between the gate regions and the channel are always kept **reverse biased** during normal operation.

- The n-type region between the two p^+ gates is the **channel** through which electrons flow from source to drain.
- Contact at one end of the bar is the **source (S)**; the contact at the other end is the **drain (D)**.

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- Because the gate is heavily doped compared with the channel, the depletion region extends mainly **into the channel**.
- In a **p-channel JFET** the bar is p-type and the gates are n^+; the polarities of all voltages and currents are reversed.
- The arrow on the gate in the symbol points **inward** for n-channel (p to n junction direction) and **outward** for p-channel.

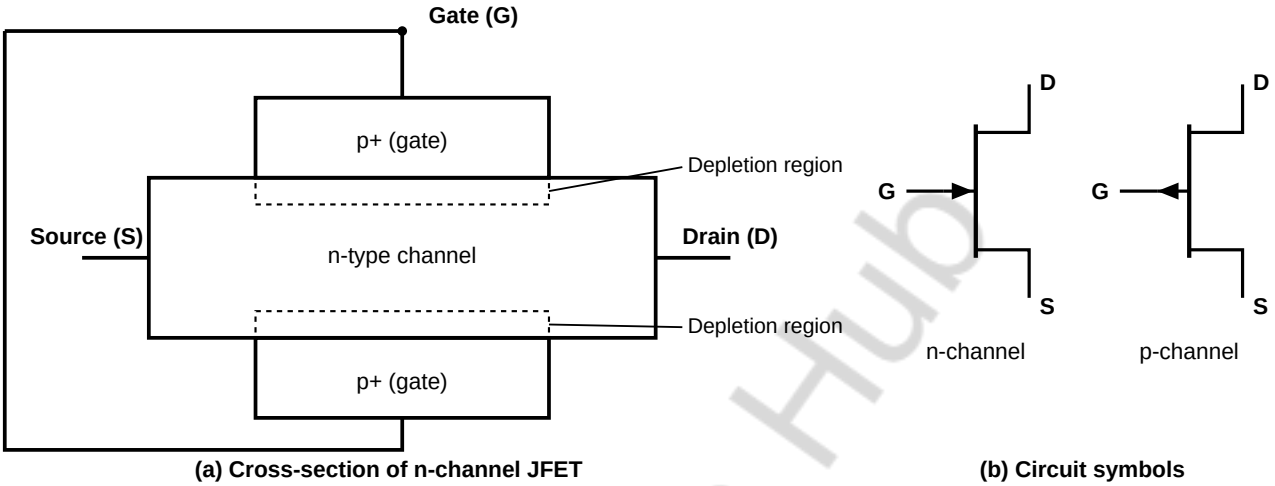

Fig. 3.1: Construction and circuit symbols of JFET

3.1.2 Operation of n-channel JFET

For normal operation, the **drain is made positive** with respect to the source ($V_{DS} > 0$) and the **gate is made negative** with respect to the source ($V_{GS} \leq 0$), which reverse biases the gate-channel junctions. The reverse biased junctions have depletion regions that are free of mobile carriers. The wider the depletion region, the narrower the conducting channel, and the smaller the drain current. Thus the gate voltage *controls* the drain current without drawing any appreciable gate current ($I_G \approx$ nanoamperes).

Case 1: $V_{GS} = 0$ and $V_{DS} = 0$

- No drain voltage, so no drain current ($I_D = 0$).
- Depletion regions are thin and of uniform width along the channel because both junctions have only the small built-in potential.

Case 2: $V_{GS} = 0$ and V_{DS} increased from zero (small values)

- Electrons flow from source to drain; the channel behaves like a **simple resistor**, so I_D increases linearly with V_{DS} (ohmic region).
- The drain end of the gate junction is reverse biased more than the source end (the voltage drop along the channel adds to the reverse bias). Hence the depletion region becomes **wedge-shaped** – wider near the drain.

Case 3: $V_{GS} = 0$ and $V_{DS} = V_P$ (pinch-off)

- As V_{DS} increases, the depletion regions widen near the drain until they almost touch. This condition is called **pinch-off**.
- The drain current at this point reaches its maximum value for $V_{GS} = 0$, called $\mathbf{I_{DSS}}$ (drain-source saturation current with gate shorted to source).
- The channel is not completely closed; a narrow conducting neck remains, and a high electric field in it sweeps carriers across.

Case 4: $V_{GS} = 0$ and V_{DS} greater than V_P

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- The pinch-off point moves slightly toward the source. The extra voltage is dropped across the short pinched-off section.
- The channel resistance rises in proportion, so I_D stays almost **constant at I_{DSS}**. This is the **saturation (pinch-off) region**, used for amplification.

Case 5: V_{GS} made negative

- The extra reverse bias widens the depletion regions, the channel narrows, and its resistance increases, so I_D **decreases**.
- Pinch-off occurs at a **lower** V_{DS}, given by $V_{DS(sat)} = V_{GS} - V_P$.
- At $V_{GS} = V_P$ (also written $V_{GS(off)}$) the depletion regions meet completely, the channel is closed and $I_D \approx 0$ – **cut-off**.

Case 6: Very high V_{DS}

- The gate-channel junction undergoes **avalanche breakdown** and I_D rises sharply. The device must never be operated in this region as it may be permanently damaged.

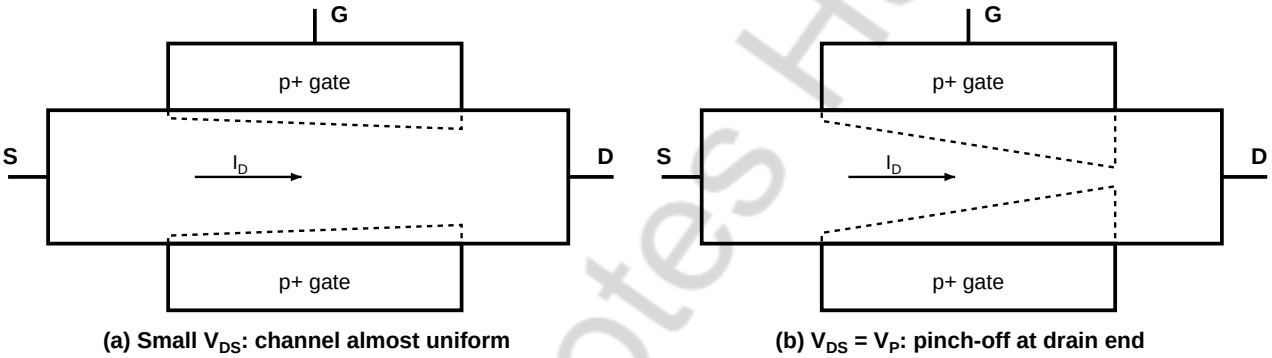

Fig. 3.2: Depletion region in an n-channel JFET (both gate regions are tied together)

3.1.3 Pinch-off Voltage (V_P)

Definition: The pinch-off voltage V_P is the value of the drain-source voltage V_{DS} (at $V_{GS} = 0$) at which the depletion regions almost touch each other and the drain current becomes **constant** (saturates at I_{DSS}). Equivalently, it is the magnitude of the gate-source voltage $\mathbf{V_{GS(off)}}$ that reduces the drain current to nearly zero.

- For an n-channel JFET, V_P is quoted as a **negative** value (e.g. −4 V) when expressed as $V_{GS(off)}$; for a p-channel JFET it is positive.
- Typical values lie between 0.5 V and 8 V (magnitude).
- V_P depends on the doping and the half-width ‘a’ of the channel: $V_P = q\, N_D\, a^2 / (2\varepsilon)$.
- At any V_{GS}, the drain voltage at which saturation begins is $V_{DS(sat)} = V_{GS} - V_P$. *Example:* if $V_P = -5$ V and $V_{GS} = -2$ V, saturation begins at $V_{DS} = -2 - (-5) = 3$ V.

$$\mathbf{V_{DS(sat)} = V_{GS} - V_P} \quad \textbf{(n-channel, } \mathbf{V_P} \textbf{ negative)}$$

3.1.4 V-I Characteristics of JFET

(a) Drain (output) characteristics

These curves show the variation of the drain current I_D with the drain-source voltage V_{DS} for different constant values of gate-source voltage V_{GS}. The topmost curve is for $V_{GS} = 0$ (maximum current, I_{DSS}); each more negative V_{GS} gives a lower curve, and the curves are closer together at higher negative V_{GS}.

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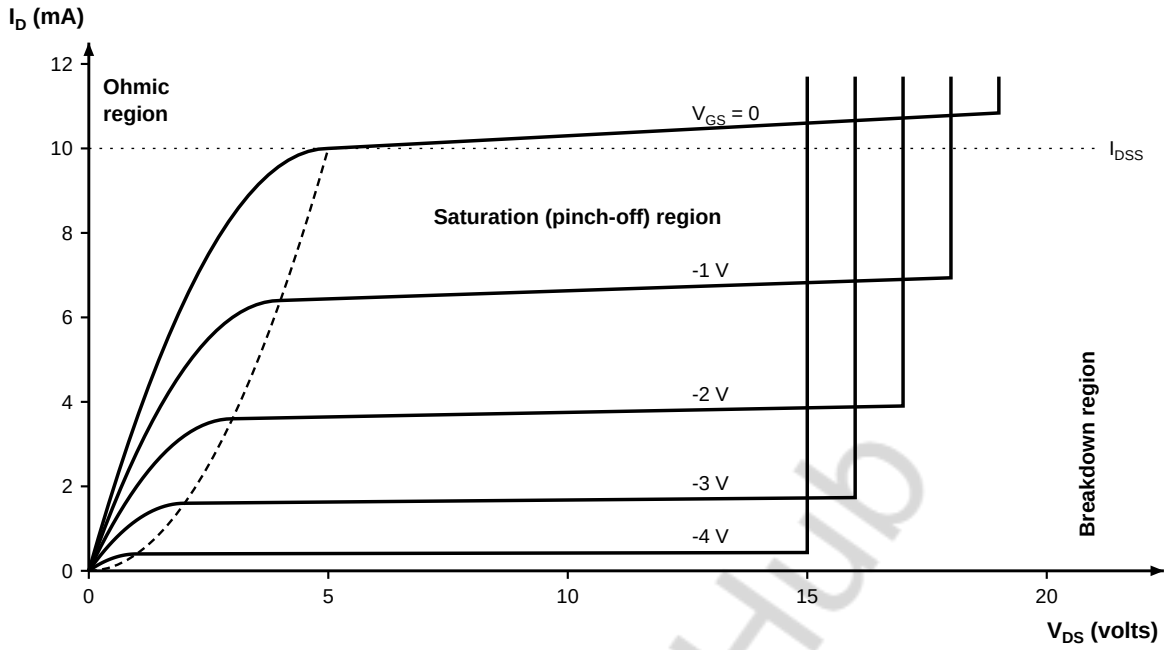

Fig. 3.3: Drain characteristics of n-channel JFET (V_P = −5 V, I_{DSS} = 10 mA). Dashed line = pinch-off locus

Region	Condition	Behaviour / Use
Ohmic (triode) region	$V_{DS} < V_{GS} - V_P$	I_D rises almost linearly with V_{DS}. JFET acts as a **voltage-variable resistor** (VVR); used in automatic gain control and analog switches.
Saturation (pinch-off) region	$V_{DS} > V_{GS} - V_P$, $V_{GS} > V_P$	I_D is nearly constant and controlled mainly by V_{GS}. The **amplifier region**.
Cut-off region	$V_{GS} \le V_P$	Channel fully closed, $I_D \approx 0$. JFET acts as an open switch (OFF).
Breakdown region	V_{DS} very large	Avalanche breakdown of gate-channel junction; I_D shoots up. Must be avoided.

(b) Transfer characteristics

The transfer characteristic is a plot of I_D against V_{GS} at a constant V_{DS} (chosen in the saturation region). It is a **parabola** that is described by **Shockley's equation**:

$$\mathbf{I_D = I_{DSS}\,(1 - V_{GS} / V_P)^2}$$

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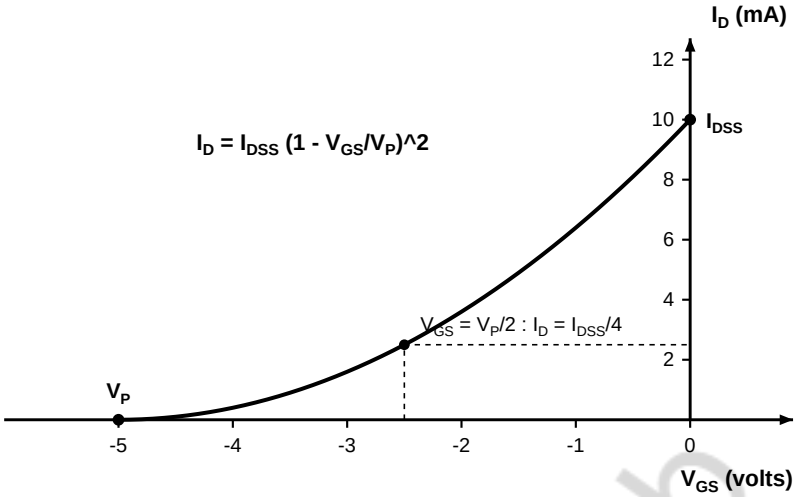

Fig. 3.4: Transfer characteristic of n-channel JFET (V_P = −5 V, I_{DSS} = 10 mA)

Important points:

- At $V_{GS} = 0$, $I_D = I_{DSS}$ (maximum drain current).
- At $V_{GS} = V_P$, $I_D = 0$ (cut-off).
- The relation is **square-law** (non-linear), which causes some distortion in amplifiers.
- The transfer characteristic can be obtained from the drain characteristics by projecting the I_D values for each V_{GS} in the saturation region.

V_{GS} / V_P	**0**	**0.25**	**0.3**	**0.5**	**0.75**	**1**
I_D / I_{DSS}	1	0.5625	0.49	0.25	0.0625	0

3.1.5 Small-Signal (AC) Parameters of JFET

When a small ac signal is applied, the JFET is characterised by three dynamic parameters – **drain resistance (r_d)**, **transconductance (g_m)** and **amplification factor (μ)**. They are obtained from the slope of the characteristic curves around the operating (Q) point.

(i) Drain (dynamic / AC) resistance, r_d

It is the ratio of the small change in drain-source voltage to the corresponding change in drain current, keeping gate-source voltage constant. It is the reciprocal of the slope of the drain characteristic.

$$\mathbf{r_d = \Delta V_{DS} / \Delta I_D \quad (V_{GS} = constant) \quad Unit: ohm (\Omega)}$$

- In the saturation region the curves are almost flat, so r_d is **very large** (typically 10 kΩ to 1 MΩ).
- In the ohmic region the slope is steep, so r_d is small.
- Also written as r_{ds} or r_o; the reciprocal is the output conductance $g_d = 1/r_d$.

(ii) Transconductance, g_m

It is the ratio of the small change in drain current to the small change in gate-source voltage, keeping drain-source voltage constant. It measures how effectively the gate voltage controls the drain current and is the slope of the transfer characteristic.

$$\mathbf{g_m = \Delta I_D / \Delta V_{GS} \quad (V_{DS} = constant) \quad Unit: siemens (S) or mho (A/V)}$$

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Differentiating Shockley's equation gives:

$$\boxed{g_m = g_{m0}\,(1 - V_{GS}/V_P) \quad \text{where} \quad g_{m0} = 2\,I_{DSS} / |V_P|}$$

- g_{m0} is the maximum transconductance (at $V_{GS} = 0$). It is also written g_{mo} or g_{fs}.
- g_m also equals $g_{m0}\,\sqrt{(I_D/I_{DSS})}$. So g_m falls as the gate is made more negative.
- Typical JFET values: 1 mS to 10 mS (much smaller than a BJT at the same current).

(iii) Amplification factor, μ

It is the ratio of the small change in drain-source voltage to the small change in gate-source voltage, keeping the drain current constant. It shows how much more effective the gate voltage is than the drain voltage in controlling the drain current.

$$\boxed{\mu = -\,\Delta V_{DS} / \Delta V_{GS} \quad (I_D = \text{constant}) \quad \text{Unit: none (pure number)}}$$

The negative sign shows that V_{GS} and V_{DS} must change in opposite directions to keep I_D constant. In practice the magnitude is used.

(iv) Relationship between r_d, g_m and μ

I_D depends on both V_{GS} and V_{DS}, that is $I_D = f(V_{GS}, V_{DS})$. For small changes, the total differential is:

$$\boxed{dI_D = (\partial I_D/\partial V_{GS})\,dV_{GS} + (\partial I_D/\partial V_{DS})\,dV_{DS} = g_m\,dV_{GS} + (1/r_d)\,dV_{DS}}$$

For constant drain current, $dI_D = 0$. Hence $g_m\,dV_{GS} + dV_{DS}/r_d = 0$, which gives $-dV_{DS}/dV_{GS} = g_m\,r_d$. By definition the left side is μ. Therefore:

$$\boxed{\mu = r_d \times g_m}$$

Parameter	Symbol	Definition	Constant	Unit
Drain resistance	r_d	$\Delta V_{DS} / \Delta I_D$	V_{GS}	Ω
Transconductance	g_m	$\Delta I_D / \Delta V_{GS}$	V_{DS}	S (mho)
Amplification factor	μ	$-\Delta V_{DS} / \Delta V_{GS}$	I_D	No unit
Relationship	μ	$r_d \times g_m$	–	–

Solved Examples

Example 1. A JFET has $I_{DSS} = 9$ mA and $V_P = -3$ V. Find I_D, g_{m0} and g_m at $V_{GS} = -1$ V.

Solution: $I_D = 9\,(1 - (-1)/(-3))^2 = 9\,(1 - 1/3)^2 = 9 \times 4/9 =$ **4 mA**. $g_{m0} = 2\,I_{DSS}/|V_P| = 2 \times 9 / 3 =$ **6 mS**. $g_m = g_{m0}(1 - V_{GS}/V_P) = 6 \times (2/3) =$ **4 mS**.

Example 2. For a JFET at constant V_{GS}, a change of 6 V in V_{DS} changes I_D by 0.3 mA. If $g_m = 3$ mS, find r_d and μ.

Solution: $r_d = \Delta V_{DS}/\Delta I_D = 6 / (0.3 \times 10^{-3}) =$ **20 kΩ**. $\mu = r_d\,g_m = 20 \times 10^3 \times 3 \times 10^{-3} =$ **60**.

3.1.6 JFET as an Amplifier (Brief)

- The JFET is biased in the saturation region so that I_D is controlled by V_{GS}.

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- A small ac signal v_{gs} produces a drain current change $i_d = g_m v_{gs}$; across the drain load R_D this gives an output voltage.
- Voltage gain of common-source amplifier: $A_v = -g_m (r_d \parallel R_D) \approx -g_m R_D$ (since r_d is much larger than R_D). The negative sign denotes 180° phase shift.
- Input resistance is very high; hence the JFET is used in input stages of instruments.

3.1.7 n-channel versus p-channel JFET

Property	**n-channel JFET**	**p-channel JFET**
Channel material	n-type semiconductor	p-type semiconductor
Gate material	p^+	n^+
Majority carriers	Electrons	Holes
V_{GS} polarity (normal)	Negative	Positive
V_{DS} polarity	Positive	Negative
Pinch-off voltage V_P	Negative	Positive
Speed / g_m	Higher (electron mobility is greater)	Lower

3.1.8 Advantages, Disadvantages and Applications of JFET

Advantages	**Disadvantages**
• Very high input impedance • Low noise • No thermal runaway, good temperature stability • No offset voltage at $I_D = 0$ (excellent chopper) • Small size, easy fabrication in ICs • Less affected by radiation	• Low gain-bandwidth product • Small gain for a given supply compared with BJT • Square-law, non-linear transfer characteristic • Gate junction can be damaged if forward biased • Spread of parameters (I_{DSS}, V_p) among devices of same type

Applications: input stage (buffer) of voltmeters, oscilloscopes and amplifiers; RF amplifiers in receivers; analog switches and choppers; voltage-variable resistors in AGC circuits; constant current sources; phase-shift oscillators; sample-and-hold circuits; low-noise preamplifiers.

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3.2 MOSFET and Concept of CMOS

3.2.0 Introduction to MOSFET

The **Metal Oxide Semiconductor Field Effect Transistor (MOSFET)** is a FET in which the gate is **insulated from the channel by a thin layer of silicon dioxide (SiO_2)**. For this reason it is also called an **Insulated Gate FET (IGFET)**. Because of the insulating layer, the gate current is practically zero (about 10^{-12} A) and the input resistance is extremely high (10^{10} to 10^{15} Ω). The gate voltage creates an electric field across the oxide that modulates the channel. MOSFETs are of two types:

- **Depletion type MOSFET (D-MOSFET)** – a channel physically exists; it can be depleted or enhanced by gate voltage.
- **Enhancement type MOSFET (E-MOSFET)** – no channel exists initially; it is induced by the gate voltage.

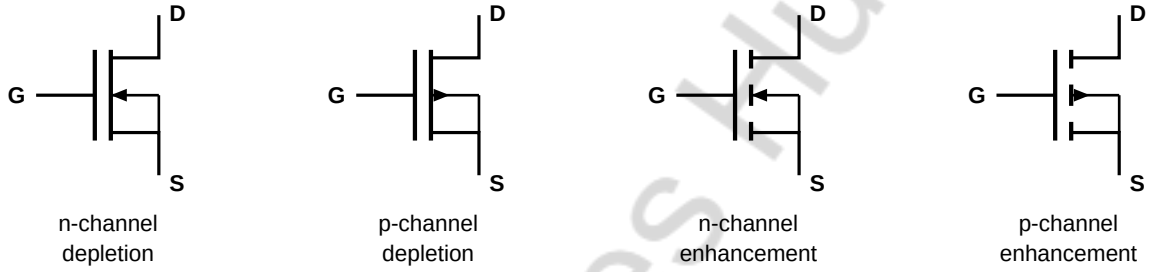

Fig. 3.5: Circuit symbols of MOSFETs (solid channel line = depletion type, broken channel line = enhancement type)

3.2.1 Depletion Type MOSFET (D-MOSFET)

Construction

- Starts with a lightly doped **p-type substrate** (also called body or bulk, terminal B).
- Two heavily doped **n^+ regions** are diffused into the substrate; they form the **source** and **drain**.
- A narrow **n-type channel** is diffused between source and drain, so a conducting path exists even at $V_{GS} = 0$.
- A thin **SiO_2 layer** (about 0.1 μm) covers the channel; a **metal gate** is deposited over the oxide. Metal contacts are made to source and drain.
- The substrate is often connected internally to the source, giving a three-terminal device. Some devices bring out the fourth terminal.

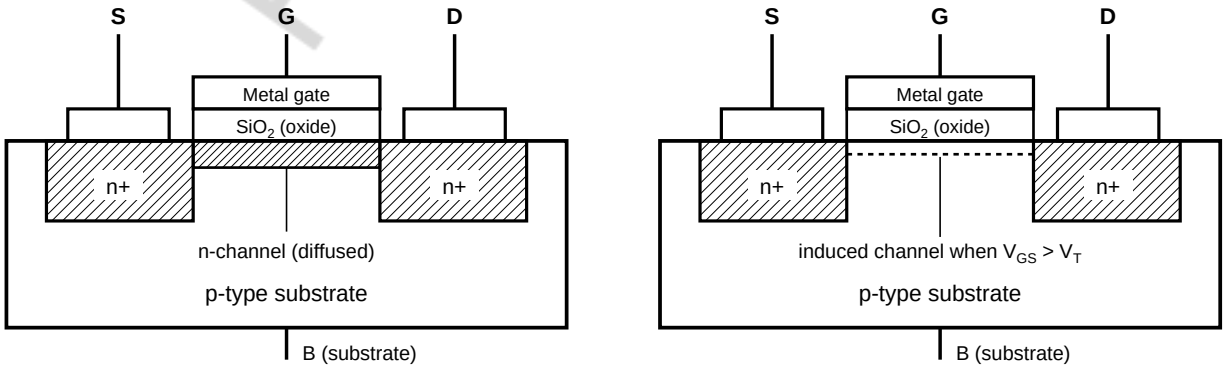

Fig. 3.6: Construction of n-channel depletion and enhancement MOSFETs

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Operation

1. **V_{GS} = 0:** With V_{DS} applied, electrons flow through the existing channel and a drain current $I_D = I_{DSS}$ flows.
2. **V_{GS} negative (depletion mode):** The negative gate repels electrons from the channel (and attracts holes), so the channel is **depleted** of carriers, becomes narrower and I_D **decreases**. At $V_{GS} = V_P$ ($V_{GS(off)}$) the channel is fully depleted and $I_D \approx 0$.
3. **V_{GS} positive (enhancement mode):** The positive gate attracts more electrons into the channel, which becomes wider and more conductive, so I_D **increases above I_{DSS}**.
4. Since the gate is insulated, the gate can be either polarity without drawing current. A D-MOSFET can therefore work in **both** depletion and enhancement modes.

The drain current in the saturation region is given by the same Shockley equation as for a JFET:

$$\mathbf{I_D = I_{DSS}\,(1 - V_{GS}/V_P)^2}$$

This equation holds for V_{GS} from V_P up to positive values (limited by maximum rated current). A **p-channel D-MOSFET** uses an n-type substrate and a p-type channel, with all polarities reversed.

3.2.2 Enhancement Type MOSFET (E-MOSFET)

Construction

- Similar to D-MOSFET, but **no channel is diffused** between source and drain: the p-type substrate extends right up to the SiO_2 layer.
- Two n^+ regions form source and drain. A metal gate sits on the oxide over the region between them.
- With no gate voltage, the source and drain are like two back-to-back p-n diodes and no current flows.

Operation

1. **V_{GS} = 0:** No channel; $I_D \approx 0$. The device is normally **OFF**.
2. **0 < V_{GS} < V_T:** The positive gate repels holes from the surface below the oxide and a depletion layer forms; still no conduction.
3. **$V_{GS} = V_T$ (threshold voltage):** The gate attracts enough minority electrons to the surface to form a thin n-type **inversion layer**, which is the **induced channel**. Conduction starts.
4. **$V_{GS} > V_T$:** The channel gets thicker and more conductive; I_D increases with V_{GS}.
5. **Large V_{DS}:** The induced channel narrows at the drain end and pinches off when $V_{DS} = V_{GS} - V_T$; beyond this I_D is nearly constant (saturation).

Threshold voltage (V_T) is the minimum gate-source voltage needed to form the induced channel. It is about 1 V to 4 V for discrete devices and about 0.4 V to 1 V in modern ICs. For a p-channel E-MOSFET, V_T and V_{GS} are negative.

Current equations (n-channel; k depends on device geometry, $k = \tfrac{1}{2}\,\mu_n C_{ox}(W/L)$):

$$\textbf{Ohmic region:}\quad \mathbf{I_D = k\,[\,2\,(V_{GS} - V_T)\,V_{DS} - V_{DS}^2\,]}$$

$$\textbf{Saturation region:}\quad \mathbf{I_D = k\,(V_{GS} - V_T)^2}$$

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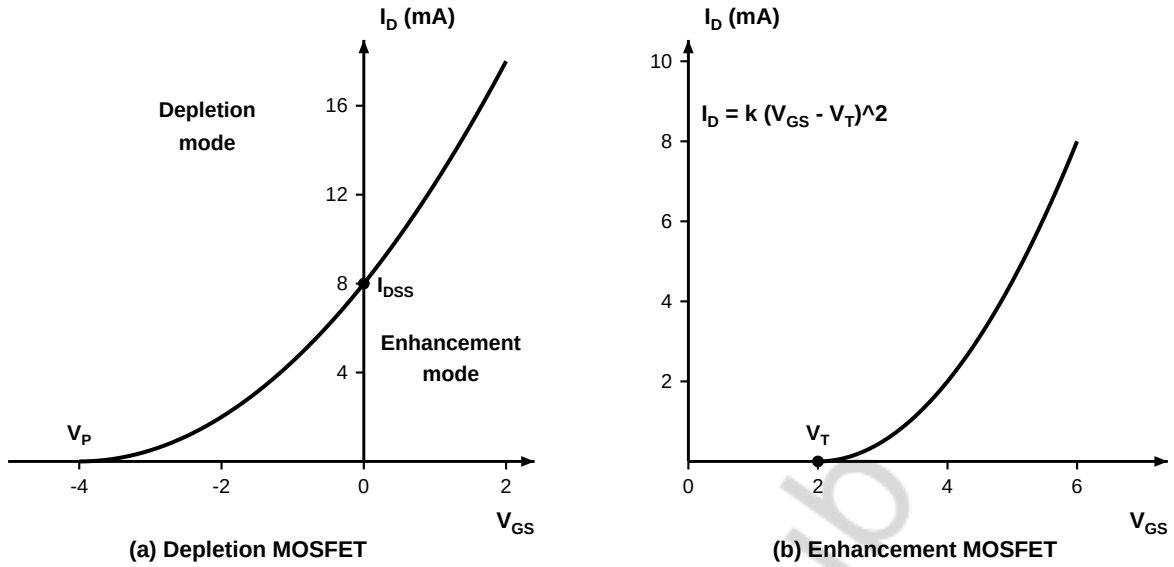

Fig. 3.7: Transfer characteristics of n-channel depletion and enhancement MOSFETs

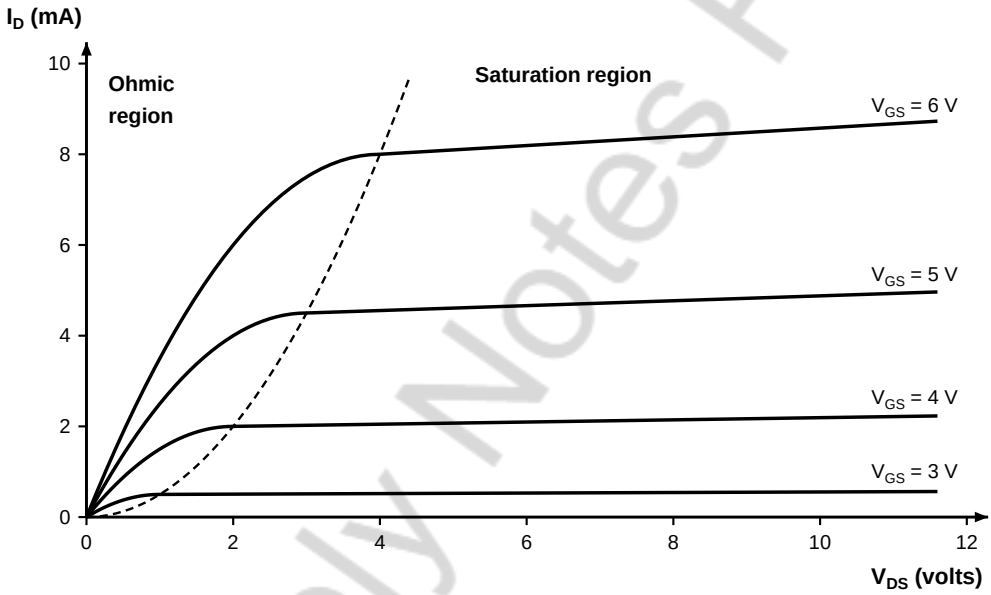

Fig. 3.8: Drain characteristics of n-channel enhancement MOSFET (V_T = 2 V, k = 0.5 mA/V^2). Dashed line = pinch-off locus

Region of E-MOSFET	Condition	Description
Cut-off	$V_{GS} < V_T$	No channel; $I_D = 0$; switch OFF.
Ohmic (triode)	$V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$	Voltage-controlled resistor; used as a closed switch.
Saturation	$V_{GS} > V_T$ and $V_{DS} \geq V_{GS} - V_T$	Constant-current region; used for amplification.

Example 3. An n-channel E-MOSFET has k = 0.5 mA/V^2 and V_T = 2 V. Find I_D in saturation at V_{GS} = 4 V.

Solution: $I_D = k (V_{GS} - V_T)^2 = 0.5 \times (4 - 2)^2 = 0.5 \times 4 =$ **2 mA**.

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3.2.3 Comparison of MOSFET Types and JFET

Parameter	Depletion MOSFET	Enhancement MOSFET
Channel	Physically present (diffused)	Not present; induced by gate voltage
I_D at $V_{GS} = 0$	Maximum (I_{DSS})	Zero (normally OFF)
Modes of operation	Both depletion and enhancement	Enhancement only
V_{GS} for n-channel	Negative and positive	Only positive ($> V_T$)
Key parameter	Pinch-off voltage V_P	Threshold voltage V_T
Drain current equation	$I_D = I_{DSS}(1 - V_{GS}/V_P)^2$	$I_D = k\,(V_{GS} - V_T)^2$
Symbol channel line	Continuous	Broken (three segments)
Typical uses	RF amplifiers, input stages	Digital logic, memories, power switching, ICs

Parameter	JFET	MOSFET
Gate construction	p-n junction (reverse biased)	Metal gate insulated by SiO_2
Input resistance	About $10^8\ \Omega$	10^{10} to $10^{15}\ \Omega$
Modes	Depletion only	Depletion and/or enhancement
Gate current	Reverse leakage (nA)	Nearly zero (pA)
Static damage	Not easily damaged	Easily damaged by static charge
Fabrication	More space per device	Very small; ideal for VLSI
Cost	Higher	Cheaper in ICs

Advantages of MOSFET

- Extremely high input impedance and very low gate current.
- Very small size and low power consumption; high packing density in ICs.
- Simple to fabricate, so used in microprocessors and memory chips.
- Fast switching, no minority-carrier storage delay.
- Enhancement type can be driven directly by logic levels.

Disadvantages of MOSFET

- The thin oxide layer is easily damaged by static electricity or excess gate voltage (typically about 20 V).
- Lower transconductance than BJT.
- Leakage current in very small geometries.

Handling precautions for MOSFETs

- Store and transport with the leads shorted by conductive foam or a shorting clip.
- Use an anti-static wrist strap and earthed soldering iron.
- Never insert or remove a MOSFET when the circuit is powered.
- Gate-protection zener diodes are built in some devices.

Applications: digital ICs, microprocessors and memories, power switching and motor drives (power MOSFETs), SMPS, audio amplifiers, RF amplifiers, analog switches, and voltage regulators.

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3.2.4 Concept of CMOS (Complementary MOS)

CMOS technology uses **both p-channel and n-channel enhancement MOSFETs** on the same silicon chip, connected in a **complementary** manner so that when one device is ON the other is OFF. In a CMOS chip, NMOS transistors are built directly in the p-type substrate while PMOS transistors are built in separate **n-wells** diffused into the substrate.

CMOS inverter (NOT gate)

The inverter has a PMOS transistor (pull-up) connected between V_{DD} and the output, and an NMOS transistor (pull-down) between the output and ground. The two gates are joined to form the input and the two drains are joined to form the output.

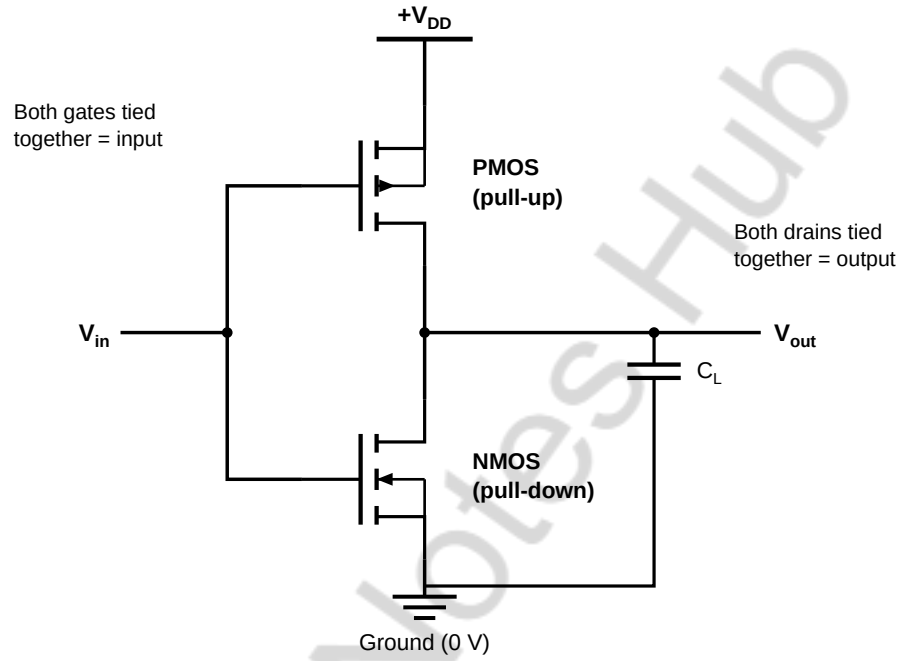

Fig. 3.9: CMOS inverter circuit

Input V_{in}	**NMOS**	**PMOS**	**Output V_{out}**
0 V (logic 0)	OFF ($V_{GS} = 0 < V_T$)	ON ($V_{GS} = -V_{DD}$)	V_{DD} (logic 1)
V_{DD} (logic 1)	ON ($V_{GS} = V_{DD}$)	OFF ($V_{GS} = 0$)	0 V (logic 0)

- In either steady state one transistor is OFF, so there is **no direct DC path** from V_{DD} to ground – static power dissipation is almost zero.
- Significant current flows only during switching, charging and discharging the load capacitance C_L. Dynamic power: $P = C_L V_{DD}^2 f$.
- The output swings the **full supply range** (rail to rail), giving excellent noise margin.

CMOS NAND and NOR (concept)

Gate	**NMOS network (pull-down)**	**PMOS network (pull-up)**
NAND	Series connection	Parallel connection
NOR	Parallel connection	Series connection

Advantages of CMOS

- Very low static power consumption (microwatts), ideal for battery-operated equipment.

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- High noise immunity (about 45% of V_{DD}).
- Very high input impedance and large fan-out.
- Wide supply range (3 V to 15 V for 4000-series; 1 V to 5 V for modern families).
- High packing density and easy scaling, suitable for VLSI.

Disadvantages of CMOS

- Needs two transistors per input, so more complex fabrication than NMOS.
- Static-sensitive; input protection is needed.
- **Latch-up** – parasitic p-n-p-n thyristor structure may trigger and cause high current.
- Dynamic power increases with switching frequency.

Applications: microprocessors and microcontrollers, SRAM/DRAM memory, 4000 and 74HC logic families, calculators, digital watches, CMOS image sensors in cameras, and almost all modern digital ICs.

Parameter	**CMOS**	**TTL**
Basic device	MOSFET	BJT
Power dissipation	Very low (static)	High (about 10 mW per gate)
Supply voltage	Wide range	Fixed 5 V
Noise margin	High	Low
Packing density	Very high	Lower
Speed	Moderate; improved in HC/HCT	Fast

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3.3 Differences between BJT and JFET

The BJT and JFET are both three-terminal amplifying devices, but they operate on very different principles. A BJT is a **current-controlled bipolar** device in which a small base current controls a large collector current. A JFET is a **voltage-controlled unipolar** device in which the gate-source voltage controls the drain current through a variable-width channel. The detailed differences are tabulated below.

S.No.	Parameter	BJT	JFET
1	Full form	Bipolar Junction Transistor	Junction Field Effect Transistor
2	Carriers	Bipolar – electrons and holes both conduct	Unipolar – only majority carriers conduct
3	Control	Current controlled (I_B controls I_C)	Voltage controlled (V_{GS} controls I_D)
4	Terminals	Emitter, Base, Collector	Source, Gate, Drain
5	Input impedance	Low (about 1–2 kΩ)	Very high (10^8 Ω or more)
6	Biasing of input junction	Base-emitter forward biased	Gate-source reverse biased
7	Input current	Appreciable base current	Negligible gate current
8	Gain parameter	Current gain β (or α)	Transconductance g_m
9	Noise	More noise	Less noise
10	Thermal stability	Poor; thermal runaway possible	Better; no thermal runaway
11	Voltage gain and bandwidth	Higher gain-bandwidth product	Lower gain-bandwidth product
12	Transfer relation	Exponential: I_C e^{V_{BE}/V_T}	Square-law: $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$
13	Switching speed	Slower (minority-carrier storage time)	Faster (no minority-carrier storage)
14	Offset voltage	Has offset voltage ($V_{CE(sat)}$) at $I_C = 0$	No offset voltage at $I_D = 0$ (good chopper)
15	Size and IC fabrication	Occupies more space	Occupies less space, suits ICs
16	Radiation effect	More affected	Less affected
17	Power handling	Better, used for high-power stages	Used for low-power/small-signal stages
18	Output characteristics	I_C versus V_{CE}	I_D versus V_{DS}
19	Cost	Cheaper	Costlier

When to choose which device

- Choose a **JFET** where very high input impedance, low noise and good temperature stability are needed (buffers, electrometers, front ends).
- Choose a **BJT** where high gain, high power or high-frequency operation is required (power amplifiers, drivers).

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Quick Revision: Important Formulas and Points

Quantity	Formula
Shockley equation (JFET, D-MOSFET)	$I_D = I_{DSS}\,(1 - V_{GS}/V_P)^2$
Saturation starts at	$V_{DS(sat)} = V_{GS} - V_P$ (JFET); $V_{DS(sat)} = V_{GS} - V_T$ (E-MOSFET)
Drain resistance	$r_d = \Delta V_{DS}/\Delta I_D$ at constant V_{GS}
Transconductance	$g_m = \Delta I_D/\Delta V_{GS}$ at constant V_{DS}
Maximum transconductance	$g_{m0} = 2\,I_{DSS}/\lvert V_P\rvert$
g_m at any bias	$g_m = g_{m0}(1 - V_{GS}/V_P) = g_{m0}\,\sqrt{(I_D/I_{DSS})}$
Amplification factor	$\mu = -\Delta V_{DS}/\Delta V_{GS}$ at constant I_D
Relationship	$\mu = r_d \times g_m$
E-MOSFET saturation current	$I_D = k\,(V_{GS} - V_T)^2$
CMOS dynamic power	$P = C_L\,V_{DD}^{\,2}\,f$
CS amplifier gain	$A_v = -\,g_m\,(r_d \parallel R_D)$

Points to remember

- FET is voltage controlled and unipolar; BJT is current controlled and bipolar.
- In a JFET the gate-channel junction is always **reverse biased**.
- $I_D = I_{DSS}$ at $V_{GS} = 0$ and $I_D = 0$ at $V_{GS} = V_P$.
- JFET works only in depletion mode; D-MOSFET works in both modes; E-MOSFET only in enhancement mode.
- V_P belongs to JFET/D-MOSFET; V_T belongs to E-MOSFET.
- MOSFET has the highest input impedance, then JFET, then BJT.
- CMOS = PMOS + NMOS in complementary pair; almost zero static power.
- MOSFETs are static sensitive and should be handled with care.

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Multiple Choice Questions (15)

Choose the correct answer. The answer key follows the questions.

Q1. A FET is a _____ device.

(A) current controlled bipolar
(B) voltage controlled unipolar
(C) current controlled unipolar
(D) voltage controlled bipolar

Q2. In an n-channel JFET, the gate region is made of _____ material.

(A) n-type
(B) intrinsic
(C) p-type (p^+)
(D) metal

Q3. The gate-source junction of a JFET is normally operated in _____ bias.

(A) reverse
(B) forward
(C) zero
(D) either forward or reverse

Q4. The gate-source voltage at which the drain current of a JFET becomes (nearly) zero is called

(A) breakdown voltage
(B) threshold voltage
(C) knee voltage
(D) pinch-off (cut-off) voltage V_P

Q5. Shockley's equation for a JFET is

(A) $I_D = I_{DSS}(1 + V_{GS}/V_P)$
(B) $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$
(C) $I_D = k(V_{GS} - V_T)^2$
(D) $I_D = I_S e^{V_{GS}/V_T}$

Q6. I_{DSS} is the drain current when

(A) $V_{GS} = V_P$
(B) $V_{DS} = 0$
(C) $V_{GS} = 0$ and the JFET is in saturation
(D) the JFET is in breakdown

Q7. The transconductance of a FET is defined as

(A) $\Delta I_D / \Delta V_{GS}$ at constant V_{DS}
(B) $\Delta V_{DS} / \Delta I_D$ at constant V_{GS}
(C) $\Delta V_{DS} / \Delta V_{GS}$ at constant I_D
(D) $\Delta I_D / \Delta V_{DS}$ at constant V_{GS}

Q8. The amplification factor μ of a JFET is equal to

(A) g_m / r_d
(B) r_d / g_m
(C) $g_m + r_d$
(D) $g_m \times r_d$

Q9. A JFET has $I_{DSS} = 10$ mA and $V_P = -4$ V. The drain current at $V_{GS} = -2$ V is

(A) 5 mA
(B) 2.5 mA
(C) 1.25 mA
(D) 10 mA

Q10. For a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V, the value of g_{m0} is

(A) 2 mS
(B) 3 mS
(C) 4 mS
(D) 8 mS

Q11. Which device has no physical channel at $V_{GS} = 0$?

(A) JFET
(B) Depletion MOSFET
(C) BJT
(D) Enhancement MOSFET

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Q12. Which of the following has the highest input impedance?

(A) MOSFET
(B) JFET
(C) BJT in CE
(D) BJT in CB

Q13. In a CMOS inverter, when the input is at logic 1, then

(A) PMOS is ON and NMOS is OFF
(B) NMOS is ON and PMOS is OFF
(C) both are ON
(D) both are OFF

Q14. The minimum gate voltage required to form the induced channel in an E-MOSFET is called

(A) pinch-off voltage
(B) breakdown voltage
(C) threshold voltage
(D) cut-in voltage of diode

Q15. A JFET is called a _____ transistor.

(A) unipolar
(B) bipolar
(C) thermal
(D) optical

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Answer Key for MCQs

Q.No.	Answer	Explanation
1	(B)	FET is voltage controlled and uses one type of majority carrier.
2	(C)	Gate p^+ regions form p-n junctions with n-channel.
3	(A)	Reverse bias gives high input resistance and controls the channel width.
4	(D)	$V_{GS(off)} = V_P$ closes the channel.
5	(B)	Square-law relationship.
6	(C)	I_{DSS} is the maximum saturation current with the gate shorted to source.
7	(A)	g_m is the slope of the transfer characteristic.
8	(D)	$\mu = r_d\, g_m$.
9	(B)	$I_D = 10\,(1 - 0.5)^2 = 2.5$ mA.
10	(C)	$g_{m0} = 2 \times 8 / 4 = 4$ mS.
11	(D)	The channel in an E-MOSFET is induced only when $V_{GS} > V_T$.
12	(A)	Insulated gate gives 10^{10}–10^{15} Ω.
13	(B)	Output is pulled to ground, giving logic 0.
14	(C)	V_T is the threshold voltage.
15	(A)	Only majority carriers take part in conduction.

Quick answer grid

Q1	Q2	Q3	Q4	Q5
B	C	A	D	B
Q6	**Q7**	**Q8**	**Q9**	**Q10**
C	A	D	B	C
Q11	**Q12**	**Q13**	**Q14**	**Q15**
D	A	B	C	A

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Descriptive (Broad) Questions (10)

Q1. Explain the construction and working of an n-channel JFET with a neat diagram. Describe what happens at pinch-off.

Q2. Draw and explain the drain (output) characteristics and transfer characteristics of an n-channel JFET. Write Shockley's equation and mention the different regions of operation.

Q3. Define pinch-off voltage, drain resistance, transconductance and amplification factor of a JFET. Derive the relationship $\mu = r_d \times g_m$.

Q4. With the help of a neat diagram, explain the construction, operation and characteristics of an n-channel depletion type MOSFET.

Q5. Explain the construction and working of an n-channel enhancement type MOSFET. What is the threshold voltage? Draw its drain and transfer characteristics.

Q6. Compare depletion type MOSFET and enhancement type MOSFET. Draw the symbols of all four types of MOSFET.

Q7. Explain the concept of CMOS. Describe the working of a CMOS inverter with the help of a circuit diagram and truth table. State its advantages and applications.

Q8. Differentiate between BJT and JFET (any ten points). Also state where each device is preferred.

Q9. A JFET has $I_{DSS} = 12$ mA and $V_P = -6$ V. Calculate (i) I_D at $V_{GS} = -3$ V, (ii) g_{m0}, and (iii) g_m at $V_{GS} = -3$ V. Also, if $r_d = 25$ kΩ, find the amplification factor.

Q10. Why is a JFET called a voltage-controlled unipolar device? Write the advantages, disadvantages and applications of JFET, and compare JFET with MOSFET.

— End of Chapter 3 —

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